

Chhatrapati Shahu Maharaj Shikshan Sanstha's

CHH. SHAHU COLLEGE OF ENGINEERING

Kanchanwadi, Paithan Road, Chhatrapati Sambhajinagar 431 011 Ph. No.: (0240) 2646373, 9922668199, 2646350 Fax: (0240) 2646222 Website: www.csmssengg.org



Approved by AICTE New Delhi, DTE (Govt. of Maharashtra) and affiliated to Dr. BATU, Lonere (Raigad).

DTE Code: 2533

Department of Electronics Engineering (VLSI Design & Technology)

List of Publications

Sr. No	Details	Type (Journal / Conference/ Proceedings / Book Chapters)
	A. Y. 2024-25	
1	Manisha L. Jadhav, Shrikant J. Honade, Anil L. Wanare, Vijay M. Sardar "Automatic Exudate Detection from Retinal Fundus Images in Diabetic Retinopathy" ISSN:970-1052, E-ISSN:SSN 2320 317X, Vol.44 No.3, P.2662-2671	Journal
2	Vaishali Dasharath Shinde, Jyoti Surve, Shrikant J. Honade, Ketaki Naik, Swarna Kuchibhotla, Sunil L. Bangare, Dhanraj Jadhav: Using Big Data Analytics for Collection Development and User Engagement" ISSN:970-1052, E-ISSN:SSN 2320 317X, Vol. 44 No. 1, P.194-207	Journal
3	Dr. Dhanraj Jadhav Dr. Vaishali Dasharath Shinde, Dr. Jyoti Surve, Dr. Shrikant J. Honade, Dr. Ketaki Naik, Dr. Swarna Kuchibhotla, Dr. Sunil L. Bangare "Breast Tumour Segmentation Using Advanced UNet with Saliency, Channel, and Spatial Attention Models" ISSN:1112-5209, Vol. 20-1s, P.488 - 497	Journal
4	Jitesh Shinde, "A Case Study on the Application of Machine Learning to the Process of Crop Forecasting," 2024 OPJU International Technology Conference (OTCON) on Smart Computing for Innovation and Advancement in Industry 4.0, Raigarh, India, 2024, pp. 1-5, doi: 10.1109/OTCON60325.2024.10688298.	Conference
	A. Y. 2023-24	
1	Vaishnavi Gathal Dr. Shrikant Honade, Srushti Gawande, Pallavi Magar "SOLID WASTE MANAGEMENT FOR SMART CITIES" ISSN:1380-7501, E-ISSN:1573-7721, Vol: 10, Page No: 1806-1809	Journal
2	Komal Choudhary Dr. Shrikant Honade, Sakshi Kalshetti, Shrinivas Adsule "CNC WRITING & DRAWING MACHINE FOR GIVEN APPLICATION" Issn: 1869-9391, Vol: 10, Page No: 1938-1942	Journal
3	Patil Ganesh, "Design and study of smart irrigation system using photovoltaic cells based smart IOT system and weather prediction system for energy and water conservation in India", International Conference on Intelligent Systems (AICERA/ICIS) Volume, Year 2023, Pages 16	Conference
4	Jitesh Shinde"Defense Strategy Security Mechanism for Sensor Network" 5th EAU Scopus & WoS indexed Int. Conf. on Cognitive Computing and Cyber Physical Systems, 5-7 April 2024.	Conference



Chhatrapati Shahu Maharaj Shikshan Sanstha's

CHH. SHAHU COLLEGE OF ENGINEERING

Kanchanwadi, Paithan Road, Chhatrapati Sambhajinagar 431 011 Ph. No. : (0240) 2646373, 9922668199, 2646350 Fax: (0240) 2646222 Website: www.csmssengg.org



5	Pankaj R. Bhusari "Real Time Face Detection and Recognition" Matlab Based Facial Recognition System published by LAP LAMBERT Academic Publishing with ISBN 978-620-6-75208-0 on 2023.	Book
	A. Y. 2022-23	
1	Patil Ganesh G, "AI Based Autonomous Room Cleaning Bot", International Conference on Futuristic Technologies (INCOFT) Volume, Year 2022, Pages 14	Conference
2	Patil Ganesh G, "Swarm robotics for ultra-violet sterilization robot" International Conference on Futuristic Technologies (INCOFT) Volume, Year 2022, Pages 15	Conference
3	Jitesh Shinde, "Neural Network Based Hand Gesture Recognition", Mukt Shabd Journal, Vol. 11, Issue 4, PP 234-244, 2022	Journal
	A.Y. 2021-22	
1	Dr.Shrikant Honade Nayan Patil, Prajakta Waghmode "ATM Theft Detection using Image Processing" ISSN:2320-9798, E-ISSN:2320-9801, Vol: 10, Page No: 1769-1771	Journal
2	Dr. Shrikant Honade Pooja Nikam, Snehal khawshi "Automated Medicine Box Detector Using Arduino Uno Microcontroller" ISSN:2320-9798, E- ISSN:2320-9801, Vol: 10, Page No: 1800-1803	Journal
3	Dr.Shrikant Honade Dipali S.Shambale, Shrikrushna Gawhale, "Automatic Question Paper Generation System", ISSN:2320-9798, E-ISSN:2320-9801, Vol: 10, Page No: 1823-1824	Journal
4	Dr. Jitesh Shinde, "On-The-Fly Key Generation Based VLSI Implementation of Advanced Encryption Standard", 6th International Conference on Communications & Electronics Systems (ICCES 2021), PPG Institute of Technology, Coimbatore, Tamil Naidu, India, IEEE XPLORE ISBN: 978-1-6654-3587-1, DOI: 10.1109/ICCES51350.2021.9489090, 8-10, July, 2021	Conference
5	Dr. Jitesh Shinde "A Power and Delay Efficient Circuit for CMOS Phase Detector and Phase Frequency Detector", 6th International Conference on Communications & Electronics Systems (ICCES 2021), PPG Institute of Technology, Coimbatore, Tamil Naidu, India, IEEE XPLORE ISBN: 978-0-7381-1405-7, DOI: 10.1109/ICCES51350.2021.9489140, 8-10, July, 2021	Conference
6	Dr. Jitesh Shinde, "Design and Analysis of FEM Novel X-Shaped Broadband Linear Piezoelectric Energy Harvester. In: Lenka T.R., Misra D., Biswas A. (eds) Micro and Nanoelectronics Devices, Circuits and Systems. Lecture Notes in Electrical Engineering, vol 781. Springer, Singapore. https://doi.org/10.1007/978-981-16-3767-4_39, ISBN: 978-981-16-3767-4, September, 2021	Book Chapter



Chhatrapati Shahu Maharaj Shikshan Sanstha's

CHH. SHAHU COLLEGE OF ENGINEERING

Kanchanwadi, Paithan Road, Chhatrapati Sambhajinagar 431 011 Ph. No. : (0240) 2646373, 9922668199, 2646350 Fax: (0240) 2646222 Website: www.csmssengg.org



7	Patil Ganesh G, "IOT Based Smart Single Phase Agriculture Motor Controller" International Research Journal of Engineering and Technology (IRJET), Volume: 09 Issue: 06 Jun 2022.	Article
8	Patil Ganesh G, "IoT-based Solar Energy Monitoring" "International Research Journal of Engineering and Technology (IRJET), Volume: 09 Issue: 06 Jun 2022.	Article
9	Patil Ganesh G, "IoT Based Smart Surveillance System" International Research Journal of Engineering and Technology (IRJET), Volume: 09 Issue: 06 Jun 2022.	Article
	A.Y. 2020-21	
1	S.R. Kadam, S.N. Pawar, akumar, 4th International Conference on Computing Methodologies and Communication [ICCMC 2020]. <i>Machine Learning</i> , 56, p.11.	Conference
2	Dr. Jitesh Shindee, "Design and Simulation of Smart Flooring Tiles using Two-Phased Triangular Bimorph Piezoelectric Energy Harvester," 2020 IEEE-HYDCON, Hyderabad, India, 2020, pp. 1-4, doi: 10.1109/HYDCON48903.2020.9242839.	Conference
3	Jitesh Shinde, "Design and Analyze of FEM novel X-Shaped Broadband Linear Piezoelectric Energy Harvester", International Conference on Micro/Nanoelectronics Devices, Circuits and Systems, National Institute of Technology Silchar, Conference Date: 29-31 January 2021	Conference
4	Dr. Jitesh Shinde, "An Improved Impulse Noise Removal VLSI Architecture Using DTBDM Method, ", Data Engineering and Communications Technology, Proceedings of ICDECT 2020, Springer Lecture Notes on Data Engineering and Communications Technologies, Volume 63, https://doi.org/10.1007/978-981-16-0081-4, ISBN 978-981-16-0080-7, ISBN 978-981-16-0081-4 (eBook), May, 2021	Book Chapter
5	Jitesh Shinde, "An Improved Impulse Noise Removal VLSI Architecture using DTBDM Method", 4th International Conference in association with Springer on Data Engineering & Communication Technology" (ICDECT-2020), Kakatiya Institute of Technology & Science, Warangal, Telangana, ISSN:2367-4512, September 25-26,2020	Conference
6	Jitesh Shinde, "Design and Simulation of Smart Flooring Tiles using Two-Phased Triangular Bimorph Piezoelectric Energy Harvester", IEEE HYDCON 2020, Hyderabad, India, DOI: 10.1109/HYDCON48903.2020.9242839 ,ISBN: 9781728149950, Sep 11-13, 2020	Conference
7	Jitesh Shinde, "Smart Hands Free Waste Compactor Bin for Public Places", AICTE Sponsored International Conference on Advanced Technologies in Electrical Engineering, Kamaraj College of Engineering	Conference



Chhatrapati Shahu Maharaj Shikshan Sanstha's

CHH. SHAHU COLLEGE OF ENGINEERING

Kanchanwadi, Paithan Road, Chhatrapati Sambhajinagar 431 011 Ph. No. : (0240) 2646373, 9922668199, 2646350 Fax: (0240) 2646222 Website: www.csmssengg.org



and Technology, K. Vellakulam, Virudhunagar, Tamil Nādu, India, ISBN: 978-93-89146-81-3,4-5th October 2019 A.Y. 2019-20 Dr. Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", ICICCT 2019 – System Reliability, Quality Control, Safety, Maintenance and Management Applications to Electrical, Electronics and Computer Science and Engineering, Springer Singapore, https://doi.org/10.1007/978-981-13-8461-5_81, Print ISBN: 978-981-13-8460-8, Online ISBN: 978-981-13-8461-5_5, June, 2019 Jitesh Shinde, "Smart Hands-Free Waste Compactor Bin for Public Places", International Journal of Digital Electronics, Vol.5: Issue 2, PP 52-58, 2019 Journal A.Y. 2018-19 G. R. Bhalekar, "Advanced Driver Assistance System (ADAS) to avoid accidents at T-Junction in India," 2018 Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), Chennai, India, 2018, pp. 1-5, doi: 10.1109/AEEICB.2018.8480946. Jitesh Shinde, "An Optimization Design Strategy for Arithmetic Logic Unit", Universal Journal of Electrical and Electronic Engineering Vol. 6(1), pp. 1 – 13 DOI: 10.13189/ujeee.2019.060101, December, 2018 Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", 14CD 2018 (International Conference on Communication Computing Control and Devices -2018), Dept. of Electronics & Comm. Engg. Institute of Technical Education & Research Siksha 'O' Anusandhan (Deemed to be University) Bhubaneswar, Orrisa, India, 17-19 December, 2018 Jitesh Shinde, "Comprehensive Review on Comparative Analysis of FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", ICIETS2018 (IEEE International Conference on Innovations in Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018 A.Y. 2016-17			
A.Y. 2019-20 Dr. Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", ICICCT 2019 – System Reliability, Quality Control, Safety, Maintenance and Management Applications to Electrical, Electronics and Computer Science and Engineering, Springer Singapore, https://doi.org/10.1007/978-981-13-8461-5_81, Print ISBN: 978-981-13-8460-8, Online ISBN: 978-981-13-8461-5_ June, 2019 Jitesh Shinde, "Smart Hands-Free Waste Compactor Bin for Public Places", International Journal of Digital Electronics, Vol.5: Issue 2, PP 52-58, 2019 Journal A.Y. 2018-19 G. R. Bhalekar, "Advanced Driver Assistance System (ADAS) to avoid accidents at T-Junction in India," 2018 Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), Chennai, India, 2018, pp. 1-5, doi: 10.1109/AEEICB.2018.8480946. Jitesh Shinde, "An Optimization Design Strategy for Arithmetic Logic Unit", Universal Journal of Electrical and Electronic Engineering Vol. 6(1), pp. 1 – 13 DOI: 10.13189/ujeee.2019.060101, December, 2018 Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", 14CD 2018 (International Conference on Communication Computing Control and Devices -2018), Dept. of Electronics & Comm. Engg. Institute of Technical Education & Research Siksha "O' Anusandhan (Deemed to be University) Bhubaneswar, Orrisa, India, 17-19 December, 2018 Jitesh Shinde, "Comprehensive Review on Comparative Analysis of FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018			
Dr. Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", ICICCT 2019 – System Reliability, Quality Control, Safety, Maintenance and Management Applications to Electrical, Electronics and Computer Science and Engineering, Springer Singapore, https://doi.org/10.1007/978-981-13-8461-5_81, Print ISBN: 978-981-13- 8460-8, Online ISBN: 978-981-13-8461-5_81, Print ISBN: 978-981-13- 8400-8, Online ISBN: 978-981-13-8461-5_81, Print ISBN: 978-981-13- 8400-8, Online ISBN: 978-981-13-8461-5_81, Print ISBN: 978-981-13- 8410-10-10-10-10-10-10-10-10-10-10-10-10-1		· · · · · · · · · · · · · · · · · · ·	
Logic Unit", ICICCT 2019 – System Reliability, Quality Control, Safety, Maintenance and Management Applications to Electrical, Electronics and Computer Science and Engineering, Springer Singapore, https://doi.org/10.1007/978-981-13-8461-5_81, Print ISBN: 978-981-13-8460-8, Online ISBN: 978-981-13-8461-5_ June, 2019 Jitesh Shinde, "Smart Hands-Free Waste Compactor Bin for Public Places", International Journal of Digital Electronics, Vol.5: Issue 2, PP 52-58, 2019 Journal A.Y. 2018-19 G. R. Bhalekar, "Advanced Driver Assistance System (ADAS) to avoid accidents at T-Junction in India," 2018 Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), Chennai, India, 2018, pp. 1-5, doi: 10.1109/AEEICB.2018.8480946. Jitesh Shinde, "An Optimization Design Strategy for Arithmetic Logic Unit", Universal Journal of Electrical and Electronic Engineering Vol. 6(1), pp. 1 – 13 DOI: 10.13189/ujeee.2019.060101, December, 2018 Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", 14CD 2018 (International Conference on Communication Computing Control and Devices -2018), Dept. of Electronics & Comm. Engg. Institute of Technical Education & Research Siksha 'O' Anusandhan (Deemed to be University) Bhubaneswar, Orrisa, India, 17-19 December, 2018 Jitesh Shinde, "Comprehensive Review on Comparative Analysis of FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", ICIETS2018 (IEEE International Conference on Innovations in Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018		A.Y. 2019-20	
Places", International Journal of Digital Electronics, Vol.5: Issue 2, PP 52-58, 2019 A.Y. 2018-19 G. R. Bhalekar, "Advanced Driver Assistance System (ADAS) to avoid accidents at T-Junction in India," 2018 Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), Chennai, India, 2018, pp. 1-5, doi: 10.1109/AEEICB.2018.8480946. Jitesh Shinde, "An Optimization Design Strategy for Arithmetic Logic Unit", Universal Journal of Electrical and Electronic Engineering Vol. 6(1), pp. 1 – 13 DOI: 10.13189/ujeee.2019.060101, December, 2018 Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", 14CD 2018 (International Conference on Communication Computing Control and Devices -2018), Dept. of Electronics & Comm. Engg. Institute of Technical Education & Research Siksha 'O' Anusandhan (Deemed to be University) Bhubaneswar, Orrisa, India, 17-19 December, 2018 Jitesh Shinde, "Comprehensive Review on Comparative Analysis of FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", ICIETS2018 (IEEE International Conference on Innovations in Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018	1	Logic Unit", ICICCT 2019 – System Reliability, Quality Control, Safety, Maintenance and Management Applications to Electrical, Electronics and Computer Science and Engineering, Springer Singapore, https://doi.org/10.1007/978-981-13-8461-5_81, Print ISBN: 978-981-13-	Book Chapter
G. R. Bhalekar, "Advanced Driver Assistance System (ADAS) to avoid accidents at T-Junction in India," 2018 Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), Chennai, India, 2018, pp. 1-5, doi: 10.1109/AEEICB.2018.8480946. Jitesh Shinde, "An Optimization Design Strategy for Arithmetic Logic Unit", Universal Journal of Electrical and Electronic Engineering Vol. 6(1), pp. 1 – 13 DOI: 10.13189/ujeee.2019.060101, December, 2018 Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", I4CD 2018 (International Conference on Communication Computing Control and Devices -2018), Dept. of Electronics & Comm. Engg. Institute of Technical Education & Research Siksha 'O' Conference Anusandhan (Deemed to be University) Bhubaneswar, Orrisa, India, 17-19 December, 2018 Jitesh Shinde, "Comprehensive Review on Comparative Analysis of FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", ICIETS2018 (IEEE International Conference on Innovations in Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018	2	Places", International Journal of Digital Electronics, Vol.5: Issue 2, PP 52-58, 2019	Journal
accidents at T-Junction in India," 2018 Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), Chennai, India, 2018, pp. 1-5, doi: 10.1109/AEEICB.2018.8480946. Jitesh Shinde, "An Optimization Design Strategy for Arithmetic Logic Unit", Universal Journal of Electrical and Electronic Engineering Vol. 6(1), pp. 1 – 13 DOI: 10.13189/ujeee.2019.060101, December, 2018 Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", 14CD 2018 (International Conference on Communication Computing Control and Devices -2018), Dept. of Electronics & Comm. Engg. Institute of Technical Education & Research Siksha 'O' Anusandhan (Deemed to be University) Bhubaneswar, Orrisa, India, 17- 19 December, 2018 Jitesh Shinde, "Comprehensive Review on Comparative Analysis of FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", ICIETS2018 (IEEE International Conference on Innovations in Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018		A.Y. 2018-19	
Unit", Universal Journal of Electrical and Electronic Engineering Vol. 6(1), pp. 1 – 13 DOI: 10.13189/ujeee.2019.060101, December, 2018 Jitesh Shinde, "An Optimization Design Approach for Arithmetic Logic Unit", I4CD 2018 (International Conference on Communication Computing Control and Devices -2018), Dept. of Electronics & Comm. Engg. Institute of Technical Education & Research Siksha 'O' Anusandhan (Deemed to be University) Bhubaneswar, Orrisa, India, 17- 19 December, 2018 Jitesh Shinde, "Comprehensive Review on Comparative Analysis of FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", ICIETS2018 (IEEE International Conference on Innovations in Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018	1	accidents at T-Junction in India," 2018 Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), Chennai, India, 2018, pp. 1-5, doi:	Conference
Unit", I4CD 2018 (International Conference on Communication Computing Control and Devices -2018), Dept. of Electronics & Comm. Engg. Institute of Technical Education & Research Siksha 'O' Anusandhan (Deemed to be University) Bhubaneswar, Orrisa, India, 17- 19 December, 2018 Jitesh Shinde, "Comprehensive Review on Comparative Analysis of FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", ICIETS2018 (IEEE International Conference on Innovations in Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018	2	Unit", Universal Journal of Electrical and Electronic Engineering Vol.	Journal
FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", 4 ICIETS2018 (IEEE International Conference on Innovations in Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018	3	Unit", I4CD 2018 (International Conference on Communication Computing Control and Devices -2018), Dept. of Electronics & Comm. Engg. Institute of Technical Education & Research Siksha 'O' Anusandhan (Deemed to be University) Bhubaneswar, Orrisa, India, 17-	Conference
A.Y. 2016-17	4	FPGA & ASIC in Multi-objective Optimization of VLSI Circuit", ICIETS2018 (IEEE International Conference on Innovations in Engineering, Technology and Sciences), NIE Institute of Technology, Mysore, Karnataka, 20-21, September, 2018	Conference
		A.Y. 2016-17	



Chhatrapati Shahu Maharaj Shikshan Sanstha's

CHH. SHAHU COLLEGE OF ENGINEERING

Kanchanwadi, Paithan Road, Chhatrapati Sambhajinagar 431 011 Ph. No. : (0240) 2646373, 9922668199, 2646350 Fax: (0240) 2646222 Website: www.csmssengg.org



1	J. R. Shinde, S. S. Salankar and S. J. Shinde, "Multi-objective optimization domino techniques for VLSI circuit," 2016 International Conference on Advances in Computing, Communications and Informatics (ICACCI), Jaipur, India, 2016, pp. 2126-2130, doi: 10.1109/ICACCI.2016.7732366, ISBN: 978-1-5090-2029-4, 21-24, September, 2016	Conference
2	Jitesh Shinde, "Sound Operated Device Control System", IJIRAS – International Journal of Innovative Research & Advanced Studies, ISSN- 2394-4404, Vol 3, Issue 13, Dec 2016	Journal
3	Jitesh Shinde,"A survey on Liquid Antenna", Advanced Trends in Engineering, Science & Humanities (ICASTESH -2016), Priyadarshini J.L. College of Engineering, Nagpur, Maharashtra, India, ISBN 978-93-81693-07-5, 15 – 17, December, 2016	Conference
4	Jitesh Shinde, "Overview & Challenges of Li-Fi", Advanced Trends in Engineering, Science & Humanities (ICASTESH -2016), Priyadarshini J.L. College of Engineering, Nagpur, Maharashtra, India, ISBN 978-93-81693-07-5, 15 – 17, December, 2016	Conference
	A.Y. 2015-16	
1	J. R. Shinde, "VLSI implementation of bit serial architecture based multiplier in floating point arithmetic," 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI), Kochi, India, 2015, pp. 1672-1677, doi: 10.1109/ICACCI.2015.7275854, ISBN: - 978-1-4799-8790-0	Conference
2	J. R. Shinde, "Multi-objective optimization for VLSI implementation of Artificial Neural Network," 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI), Kochi, India, 2015, pp. 1694-1700, doi: 10.1109/ICACCI.2015.7275857, ISBN: - 978-1-4799-8790-0	Conference
3	Jitesh Shinde, "Multi-objective Optimization Approach for VLSI Implementation of FIR Filter", IOSR-Journal of VLSI Signal Processing, Vol 5, Issue 6, Ver. II, PP 108-120, e-ISSN: 2319 – 4200, p-ISSN No.: 2319 – 4197, Nov-December, 2015	Journal
	A.Y. 2014-15	
1	J. R. Shinde and S. Salankar, "Multi-objective Optimization for VLSI Circuits," 2014 International Conference on Computational Intelligence and Communication Networks, Bhopal, India, 2014, pp. 1037-1041, doi: 10.1109/CICN.2014.218.	Conference



Chhatrapati Shahu Maharaj Shikshan Sanstha's

CHH. SHAHU COLLEGE OF ENGINEERING

Kanchanwadi, Paithan Road, Chhatrapati Sambhajinagar 431 011 Ph. No. : (0240) 2646373, 9922668199, 2646350 Fax: (0240) 2646222 Website: www.csmssengg.org



	Patil Ganesh G, "A Study on ARM Cortex M3 Based Hardware	
2	Debugging", at IJSRD - International Journal for Scientific Research &	Article
	Development Vol. 3, Issue 03, 2015 (ISSN: 2321-0613).	Article
	Jitesh Shinde, "Multi-objective Optimization for VLSI Circuits", IEEE	
	International Conference on Computational Intelligence &	
3	Communication Networks", Kolkata, West Bengal, India, Print ISBN: -	Conference
	978-1-4799-6928-9, DOI: 10.1109/CICN.2014.218 November 14-16,	Conference
	2014	
	"Real time face detection and recognition system" at international	
4	conference on advances in computer science, electronics and	
4	communication technologies in Bangkok at Thailand under in absentia on	Conference
	25 January 2014	
	"Real time face detection and recognition system" in cosmic journal	
5	specifically in international journal of computer science and technology	Journal
	(IJCST, Vol. 5 Issue Spl 1, January-March, 2014).	Journal