Dr. Babasaheb Ambedkar Technological University (Established a University of Technology in the State of Maharashtra)
(under Maharashtra Act No. XXIX of 2014)
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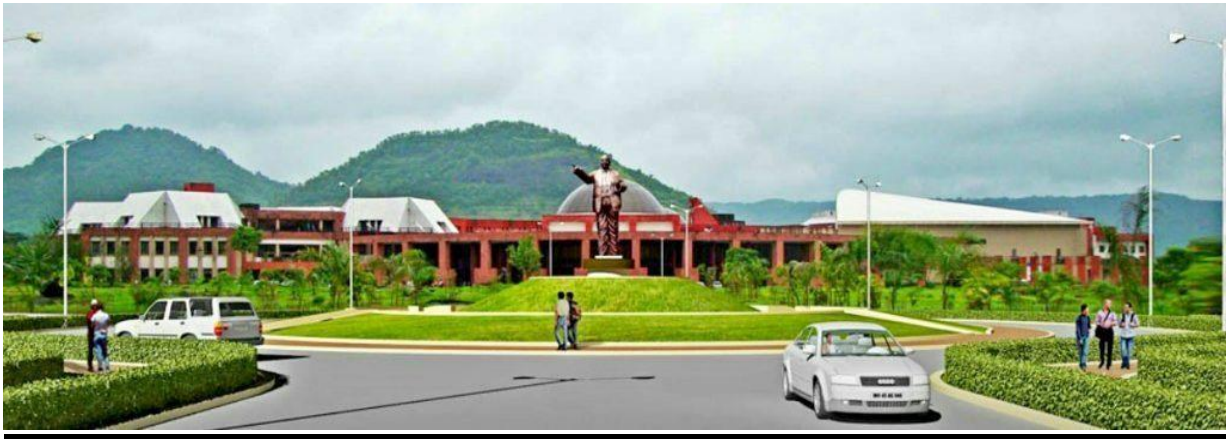
PROPOSED CURRICULUM POST GRADUATE PROGRAMME

M. TECH

Electronics and Communication (VLSI Design)

Two Year (Four Semester) Course

WITH EFFECT FROM THE ACADEMIC YEAR 2023-2024



M.Tech Electronics and Communication (VLSI Design)

Very Large Scale Integrated (VLSI) Circuit Design is setting the standard for the progression of technology. M. Tech Electronics and Communication (VLSI Design) discourses the modern design technology using computer-aided design (CAD) tools and allied hardware. The course focuses on learning the principles of VLSI design & fabrication, considering the complete design flow and evolving capability to design CMOS chip layout for industrial applications. The programme sets the basis for career prospects in foremost VLSI design industries, research laboratories, and alleged national and international organizations.

Objectives:

I. To serve the society and nation, by providing high quality engineering educationalprograms to the students, engaging in research and innovations that will enhance the skill and knowledge and assisting the economic development of the region, state, and nation through technology transfer.

II. To equip the postgraduate students with the state of the art education through research and collaborative work experience/culture to enable successful, innovative, and life-long careers in VLSI Design

III. To encourage the post-graduates students, to acquire the academic excellence and skills necessary to work as VLSI Design professional in a modern, ever-evolving world.

IV. To provide the broad understanding of social, ethical and professional issues of contemporary engineering practice and related technologies, as well as professional, ethical, and societal responsibilities.

V. To inculcate the skills for perusing inventive concept to provide solutions to industrial, social or nation problem.

Outcomes

I. Students of this program will have ability to apply knowledge of mathematics, sciences and engineering to VLSI design related problems.

II. Postgraduate students will gain an ability to design and conduct experiments, as well as to analyze and interpret data/results.

III. Learners of this program will built an ability to design and develop a system,

components, devices, or process to meet desired needs.

IV. Masters students of this program will have an ability to work on multi-disciplinaryteams and also as an individual for solving issues related to VLSI domain.

V. Learners of this program will have an ability to identify, formulate, and solve Engineering problems by applying mathematical foundations, algorithmic principles, and VLSI design theory in the modeling and design of electronics and communication systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

VI. Postgraduate students will have an ability to communicate effectively orally andin writing and also understanding of professional and ethical responsibility.

VII. Postgraduate students will have an ability to use the techniques, skills, and modernengineering EDA tools necessary for VLSI design practices.

VIII. Learners of this program will have an ability to evaluate Electronics and communication Engineering problems with cost effectiveness, features, and user friendliness to cater needs for innovative product development.

IX. Postgraduate students will have an ability to solve contemporary social and industrial problems by engaging in life-long learning.

Babasaheb Ambedkar Technological University
Teaching and Examination Scheme for
M.Tech. Electronics and Communication (VLSI Design) w.e.f. 2023-24

Sr. No.	Course Code	Name of the Course	Hours/Week			Credit	Examination scheme				
							Theory		IA	PR/ OR	TOTAL
			L	P	T		TH	Test			
First Semester											
01	MTVLSIC101	RTL Simulation & Synthesis with PLDs	03	--	1	04	60	20	20	--	**100**
02	MTVLSIC102	Embedded Systems	03	--	1	04	60	20	20	--	**100**
03	MTVLSIC103	Advanced Digital Signal Processing	03	--	1	04	60	20	20	--	**100**
04	MTVLSIE114	Elective-I	03	--	--	03	60	20	20	--	**100**
05	MTVLSIE125	Elective-II	03	--	--	03	60	20	20	--	**100**
06	MTVLSIC106	Communication Skills	02	--	--	02	--	--	25	25	**50**
07	MTVLSIL107	PG Lab-I*	--	03	--	02	--	--	25	25	**50**
		Total for Semester I	**17**	**03**	**03**	**22**	**300**	**100**	**150**	**50**	**600**
Second Semester											
01	MTVLSIC201	Analog & Digital VLSI Design	03	--	1	04	60	20	20	--	**100**
02	MTVLSIC202	VLSI Design Verification & Testing	03	--	1	04	60	20	20	--	**100**
03	MTVLSIE233	Elective-III	03	--	--	03	60	20	20	--	**100**
04	MTVLSIE244	Elective- IV	03	--	--	03	60	20	20	--	**100**
05	MTVLSIE255	Elective-V- (Open to all)	03	--	--	03	60	20	20	--	**100**
06	MTVLSIS206	Seminar-I	--	04	--	02	--	--	50	50	**100**
07	MTVLSIP207	Mini-Project	--	04	--	02	--	--	50	50	**100**
		Total for Semester II	**15**	**08**	**02**	**21**	**300**	**100**	**200**	**100**	**700**

*** PG Lab-I –Practical shall be based on courses of first semester.**

 # Student has to choose this course either from NPTEL/MOOC pool and submission of course completion certificate is mandatory.

Elective-I:

- Image Processing & Computer Vision
- Programming Language for Embedded Systems
- Mixed Signal Design
- RF Engineering
- VLSI Signal Processing

Elective-II:

- Parallel Processing
- System Design with Embedded Linux
- CAD of Digital Systems

- Smart Antennas
- ASIC Design

Elective-III:

- Memory Technologies
- System On-Chip Design
- Low Power VLSI Design
- Computer networks
- Real Time Embedded Systems

Elective-IV:

- Network Security & Cryptography
- Physical Design Automation
- Reconfigurable Computing
- VLSI Sub-system Design
- Fault Tolerant Digital System Design

Elective-V (Open):

- Artificial Intelligence & Machine learning
- Operation Research
- Business Analytics
- Composite Materials
- Industrial Safety

Sr. No.	Course Code	Name of the Course	Hours/Week			Credit	Examination scheme				
							Theory		IA	PR/ OR	TOTAL
			L	P	T		TH	Test			
Third Semester											
01	MTVLSIC301	Research Methodology & Intellectual Property Rights (Self Study)#	--	--	--	02	--	--	50	50	**100**
02	MTVLSIP302	Project-I	--	--	--	10	--	--	50	50	**100**
		Total for Semester III	**--**	**--**	**--**	**12**	**--**	**--**	**100**	**100**	**200**
Fourth Semester											
01	MTVLSIP401	Project-II	--	--	--	20	--	--	100	100	**200**
		Total for Semester IV	**--**	**--**	**--**	**20**	**--**	**--**	**100**	**100**	**200**
GRAND TOTAL											**1700**

SEMESTER-I

MTVLSIC101: RTL Simulation and Synthesis with PLDs

Weekly Teaching Hours: 4	TH: 03			Tut: 01
Scheme of Marking	TH: 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

1	To introduce Verilog HDL for the design and functionality verification of a digital circuit.
2	To understand the design of data path and control circuits for sequential machines
3	To introduce the concept of realizing a digital circuit using PLDs

Course Outcomes:

At the end of course, students should:

CO1	Familiarize with Finite State Machines, RTL design using reconfigurable logic.
CO2	Design and develop IP cores and Prototypes with performance guarantees
CO3	Use EDA tools like Cadence, Mentor Graphics and Xilinx.
CO4	Understand the Static Timing Analysis and clock issues in digital circuits
CO5	Verify the functionality of the digital designs using PLDs.
CO6	Appreciate the analysis of finite state machine of a controlling circuit

UNIT-I:

Basics of Verilog HDL: Importance of HDLs, Lexical Conventions of Verilog HDL. Introduction to Verilog HDL, Abstraction levels, basic concepts, Verilog primitives, keywords, data types, nets and registers, Verilog Modules and ports, Logical Operators, Bitwise and Reduction Operators, Concatenation and Conditional Operators, Relational and Arithmetic, Shift and Equality Operators, Operator Execution Order **(7hrs)**

UNIT-II:

Verilog Gate level modeling: Built in primitive gates, switches, gate delays. Data flow modeling: Continuous and implicit continuous assignment, delays. Behavioral modeling: Procedural constructs, Control and repetition Statements, delays, function and tasks. Always Block, Flow Control, If-Else, Case, Cases, While Loop, For Loop, Repeat **(7hrs)**

UNIT-III:

Logic Synthesis, RTL Synthesis, High-Level Synthesis, Synthesis Design Flow, Design and Analysis of Combinational Circuits, Flip flops, Arithmetic Circuits, Encoder, Decoder, De-Multiplexer Circuits, Multiplexer Circuits and their Implementation Using Verilog, Design of a 4-Bit Comparator, Design of a 4- Bit ALU. **(7hrs)**

UNIT-IV:

Programmable Logic Devices, Introduction to ASIC Design Flow, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection. **(7hrs)**

UNIT-V:

Digital Design using PLDs: ROM, PLA, PAL- Registered PALs, Configurable PALs, and GAL. CPLDs: Features, architecture and applications using complex programmable logic devices. **(6hrs)**

Unit VI: FPGAs: Xilinx XC 4000 Features and Architectures, Configurable Logic Blocks

(CLBs), Input Output Blocks (I/OB), Block RAM, Programming Interconnects, Digital Clock Manager (DCM). **(6hrs)**

TEXT BOOKS:

1. Verilog HDL, A Guide to Digital Design and Synthesis Samir Palnitkar, 2nd Edition, 2003
2. Bhasker, Jayaram. "Verilog HDL Synthesis: A Practical Primer", Star Galaxy Publishing, 2008.
3. S.M. Trimberger, "Field-Programmable Gate Array Technology," Springer Science & Business Media,2012
4. I Grout, "Digital Systems Design with FPGAS and CPLDS," Elsevier, 2011
5. Modern Digital Electronics P Jain, 3rd Edition, TMH, 2003
6. Data Sheets for CPLD & FPGA architectures, 1996.

REFERENCES:

1. Donald D Givone, "Digital principles and Design", TMH, 2016
2. Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books, 2002.
3. Richard S. Sandige, "Modern Digital Design", MGH, International Editions, 1990
4. W.Wolf, "FPGA-Based System Design," Pearson education, 2004

MTVLSIC102: Embedded Systems

Weekly Teaching Hours:04	TH: 03			Tut: 01
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

1	Understand the concept of embedded system, different components of embedded system and their interactions
2	Explore the architecture and instruction set of ARM processor.
3	Explore the architecture, Task Management, scheduling and inter-process communication in real time operating systems.

Course Outcomes:

At the end of course, students should:

CO1	Recognize the need of Embedded System and System on Chip (SoC).
CO2	Identify the internal Architecture and perform the programming of ARM processor.
CO3	Apply the concept of Thumb mode operation and interfacing of coprocessors in an embedded system.
CO4	Interface AMBA bus architecture, various HW peripherals in embedded systems and how memory mapping can be done.
CO5	Analyze the need of Real time Operating System (RTOS) in embedded systems
CO6	Able to design embedded systems applications.

Unit 1: Introduction to Embedded Systems:

Background and History of embedded systems, Definition and Classification, Characteristic of embedded system, Von-Neumann and Harvard architectures, Processor design trade-offs, CISC and RISC architectures, Programming languages for embedded systems, Embedded Systems on a Chip (SoC) and the use of VLSI designed circuits. **(6hrs)**

Unit 2: ARM Processor Fundamentals and pipeline structure:
ARM Architecture, ARM General purpose Register set and GPIO's, CPSR, Pipeline, Exceptions, Interrupts, Vector Table, ARM processors family, ARM core data flow model, ARM 3 stage Pipeline, ARM family attribute comparison. ARM 5 stage Pipeline, Pipeline Hazards, Data forwarding. **(6hrs)**

Unit 3: ARM7TDMI Processor assembly instructions:
ARM instruction set. ARM programming in Assembly, in C and C++ Instruction Scheduling, Conditional Execution, Looping Constructs, Bit Manipulation, Exception and Interrupt Handling. Thumb state, Thumb instruction set, Thumb Programmers model, Thumb Applications, ARM coprocessor interface and Instructions, Coprocessor Instructions. **(7hrs)**

Unit 4: ARM tools and Peripherals:
ARM Development Environment, Arm Procedure Call Standard (APCS), Example C/C++ programs, Embedded software Development, Protocols (I2C, SPI), GPIO, ARM systems with MPU, Memory Protection Unit (MPU). Physical vs Virtual Memory, Paging, Segmentation. AMBA Overview, Typical AMBA Based Microcontroller, AHB bus features, AHB Bus transfers, APB bus transfers, APB Bridge. **(7hrs)**

Unit 5: Real Time Operating Systems (RTOS):
Architecture of an RTOS (MicroC/OS-II, Vx Works), important features of RTOS, Locks and Semaphores, Operating System Timers and Interrupts, Exceptions, Tasks: Introduction, Defining a task, Task states and scheduling, Task structures, Synchronization, Communication and concurrency, Kernel objects: Semaphores, Queues. **(7hrs)**

Unit 6: Advanced Microcontroller:
Introduction to RENESAS Microcontroller (RL78/G13), features and architecture of RENESAS Microcontroller. Different power modes, Advantages and application of the RZ Family. **(7hrs)**

TEXT BOOKS:

1. Steve Furber, "ARM System-on-Chip Architecture, Second Edition, PEARSON, 2013.
2. Andrew N. Sloss, ARM System Developer's Guide Designing and Optimizing System Software, Morgan Kaufman Publication (2010).
3. Embedded Systems, (2nd ed.) by Raj Kamal (McGraw Hill), 2008.
4. Introduction to Embedded Systems by K.V. Shibu (McGraw Hill), 2009.

REFERENCES:

1. Simon, D.E., Embedded Software Primer, Dorling Kindersley (2005).
2. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008.
3. User manual of Raspberry pi and Red Pitaya embedded board.
4. Michael McRoberts, Beginning Arduino, Technology in action publications, 2nd Edition.
5. RENESAS Microcontroller :- www.renesas.com

MTVLSIC103: Advanced Digital Signal Processing

Weekly Teaching Hours:04	TH: 03			Tut: 01
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

1	To provide graduates strong mathematical skills and in depth knowledge in signal theory to analyze and solve complex problems in the domain of signal processing
2	To instill research skills and bring in optimal solutions to signal processing and allied application areas using modern technology and tools that are technically sound, economically feasible and socially acceptable.

Course Outcomes:

At the end of course, students should:

CO1	Understand and analyze- DTFT, DFT, and FFT.
CO2	Create & Evaluate Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) Filters
CO3	Understand the fundamentals of multi rate signal processing and its application
CO4	Apply the knowledge of DSP processor for various real time applications.
CO5	Use the concept of wavelet transform for signal processing applications.
CO6	Understand the concept of adaptive filters.

UNIT- 1: Overview of DSP & Basics of Filter Design:

Convolution, correlation, Z-transform, DTFT, DFT and their properties, and DIT-FFT and DIF-FFT algorithm. HPF, BPF, BRF filters, Structures of FIR & IIR filters. **(6hrs)**

UNIT – II: Filter Design:

Analog filter design: Butterworth and Chebyshev filter to 2^{nd} order approximations, Discrete time IIR filter from analog filter, IIR filter design by Impulse Invariance, Bilinear transformation, Approximation of derivatives, Linear phase FIR filter, Filter design using windowing techniques and Frequency sampling techniques. Implementation of Filter using filter structure. **(7hrs)**

UNIT – III: Multi-rate Digital Signal Processing:

Decimation & Interpolation, Linear filtering with decimation and interpolation, Poly-phase filters, Filter banks, sub-band processing, Decimated filter banks, Uniform DFT filter banks, Quadrature mirror filters. **(6hrs)**

UNIT – IV: DSP Processors and its Application:

Issues involved in DSP processor design, Features of TMS 320C67XX, Architecture of TMS 320C67XX, Memory Organization, Addressing Modes, Pipeline operations, Assembly language instructions, Applications of DSP to Biomedical Signal Processing, Speech signal processing, Radar signal processing. **(7hrs)**

UNIT – V: Wavelets:

Time-Frequency Analysis and Continuous Wavelet Transform, an introduction to Hilbert Space Theory, Wavelet Properties, Discrete Wavelets, Scaling Function, Sub-band Coding, Discrete Wavelet Transform. **(7hrs)**

UNIT – VI: Adaptive Signal Processing:
Adaptive filter, Main components of the adaptive filter, Basic Wiener filter theory, the basic LMS adaptive algorithm, Practical limitations of the basic LMS algorithm, Recursive Least Square Algorithm, Limitations. Application- Adaptive filter as a Noise Canceller in fetal ECG. **(7hrs)**

TEXT BOOKS:
1. 'Digital Signal Processing Principles, Algorithm and Applications", J. G. Proakis and D. G. Manolakis, Fourth Ed Prentice Hall 1997.
2. "A Course in Digital Signal Processing ", Boaz Porat John Wiley & Sons.
3. "Digital Signal Processing", Nagoor Kani, Tata-Mc-GrawHill.Publication.
4. "Digital Signal Processors", B. Venkatramani and M. Bhaskar, nd Ed., Mc-Graw Hill.
5. "Wavelet Transforms: Introduction to Theory and Applications", Bopardikar and Rao.

REFERENCES:
1. "Digital Signal Processing- A Computer based Approach", Sanjit K. Mitra, 4th Ed, Mc-Graw Hill.
2. "Discrete Time Signal Processing : A Practical Approach", E.C. Ifeacher & B.W. Jarvis Pearson Education 3rd Edition.
3. "Digital Signal Processing", Thomas J. Cavicchi, John Wiley
4. "DSP Handbook", Vijay Medisetti & D.B. Williams, CRC Press
5. "Discrete Wavelet Transform', Robi Polikar.
6. "Wavelets and Subband Coding", Valterli & Kovaceric, PHI.
7. "Analog Devices & Texas Instruments", Users Manuel of TMS320C4X and ADSP 2106X.

MTVLSIC106 : Communication Skills

Weekly Teaching Hours		TH: 02	Credit: 02	Tut:-
Scheme of Marking	TH: 60	IA: 25	PR/OR: 25	Total: 50

Course Objectives:

A To become more effective confident speakers and deliver persuasive presentations
B To develop greater awareness and sensitivity to some important considerations in interpersonal communication and learn techniques to ensure smoother interpersonal relations

Course Outcomes:

CO1: Learner will be able to understand the fundamental principles of effective business communication
CO2: Learner will be able to apply the critical and creative thinking abilities necessary for effective communication in today's business world
CO3: Learner will be able to organize and express ideas in writing and speaking to produce messages suitably tailored for the topic, objective, audience, communication medium and context
CO4: Learner will be able to demonstrate clarity, precision, conciseness and coherence in your

use of language
CO5: Learner will be able to become more effective confident speakers and deliver persuasive presentations

Course Contents:

UNIT I
Introduction to communication, Necessity of communication skills, Features of good communication, Speaking skills, Feedback & questioning technique, Objectivity in argument **(6hrs)**

UNIT II
Verbal and Non-verbal Communication, Use and importance of non-verbal communication while using a language, Study of different pictorial expressions of non-verbal communication and their analysis **(6hrs)**

UNIT III
Academic writing, Different types of academic writing, Writing Assignments and Research Papers, Writing dissertations and project reports **(7hrs)**

UNIT IV
Presentation Skills: Designing an effective Presentation, Contents, appearance, themes in a presentation, Tone and Language in a presentation, Role and Importance of different tools for effective presentation **(7hrs)**

UNIT V
Motivation/ Inspiration: Ability to shape and direct working methods according to self-defined criteria Ability to think for oneself, Apply oneself to a task independently with self-motivation, Motivation techniques: Motivation techniques based on needs and field situations **(7hrs)**

UNIT VI
Self Management, Self Evaluation, Self discipline, Self criticism, Recognition of one's own limits and deficiencies, dependency, etc. Self Awareness, Identifying one's strengths and weaknesses, Planning & Goal setting, Managing self-emotions, ego, pride, Leadership & Team Dynamics **(7hrs)**

Textbooks / References:

1. Mitra, Barun, "Personality Development and Soft Skills", Oxford University Press, 2016

2. Ramesh, Gopalswamy, "The Ace of Soft Skills: Attitude, Communication and Etiquette for Success," Pearson Education, 2013

3. Covey, Stephen R., "Seven Habits of Highly Effective People: Powerful Lessons in Personal Change".

4. Rosenberg Marshall B., "Nonviolent Communication: A Language of Life".

MTVLSIL107: PG LAB-1

Weekly Practical Hours:03	Credit: 02			Tut: -
Scheme of Marking	TH: -	PR/OR: 25	IA: 25	Total: 50

Practical's of the Lab - I shall be based on the courses of first semester. The lab work shall consists of hands on experiments on the different software and hardware platforms related to the syllabus.

SEMESTER-II

MTVLSIC201: Analog & Digital VLSI Design

Weekly Teaching Hours: 4	TH: 03			Tut: 01
Scheme of Marking	TH: 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

1	To teach fundamentals of CMOS Digital integrated circuit design such as importance of Combinational MOS logic circuits, and Sequential MOS logic circuits.
2	To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.
3	Basic design concepts, issues and tradeoffs involved in analog IC design are explored
4	To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op-Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.

Course Outcomes:

At the end of course, students should:

CO1	Gain the knowledge about Technology scaling & NMOS Fabrication process.
CO2	Appreciate the trade-offs involved in analog integrated circuit design.
CO3	Understand and appreciate the importance of noise and distortion in analog circuits.
CO4	Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
CO5	Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.
CO6	Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.

Analog CMOS Design:

UNIT-I:

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell. **(7hrs)**

UNIT-II:

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise **(6hrs)**

Unit III:

Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques. **(6hrs)**

Digital CMOS Design:

UNIT-IV:

Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process.

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their Evaluation, Dynamic behavior, Power consumption. **(8hrs)**

UNIT-V:

Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logical effort, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic. **(6hrs)**

UNIT-VI:

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc. **(7hrs)**

TEXT BOOKS:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
3. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.

REFERENCES:

1. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
2. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
3. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design",TMH, 3rd Edition.
4. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

MTVLSIC202: VLSI Design Verification & Testing

Weekly Teaching Hours: 4	TH: 03			Tut: 01
Scheme of Marking	TH: 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

1	In this course students will learn test economics, fault modelling, logic and fault simulation, ATPG concepts for combinational and sequential circuits.
2	Students will also able to write testbench for the complex VLSI design using System Verilog.

Course Outcomes:

At the end of course, students should:

CO1	Acquire knowledge about fault modelling and collapsing.
CO2	Learn about various combinational automatic test pattern generation techniques.
CO3	Learn about various sequential automatic test pattern generation techniques.
CO4	Analyze different memory faults and its testing methods.
CO5	Develop the verification plan for the small to complex VLSI designs.
CO6	Develop testbench using HVL for testing and verification of VLSI designs.

UNIT-I:

Role of testing in VLSI design, issues in test and verification of complex chips, VLSI test process and equipment, Test economics, Yield analysis and product quality.
Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance. **(8hrs)**

UNIT-II:

Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef, Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width. **(8hrs)**

UNIT-III:

ATPG for combinational circuits: D-Algorithm, Boolean Difference, PODEM, Random, Exhaustive and Weighted Test Pattern Generation, Aliasing and its effect on Fault coverage. ATPG for sequential circuits: ATPG for Single-Clock Synchronous Circuits, Time frame expansion method, Simulation-Based Sequential Circuit ATPG. **(8hrs)**

UNIT-IV:

Memory testing and BIST: Permanent, Intermittent and pattern sensitive faults, March test notion, Memory testing using march tests, PLA testing, Ad-Hoc DFT methods, Scan design, Partial scan design, Random logic for BIST, Memory BIST. **(6hrs)**

UNIT-V:

Verification: Design verification techniques based on simulation, Analytical and formal approaches, Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation. **(6hrs)**

Unit VI:

Hardware verification language: Introduction to System Verilog, Development of stimulus generator, Monitor and complete test bench using System Verilog. **(6hrs)**

TEXT BOOKS:

1. Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers

REFERENCES:

1. M. Abramovici, M. Breuer, and A. Friedman, Digital System Testing and Testable Design, IEEE Press, 1994
2. Diraj K. Pradhan, "Fault Tolerant Computer System Design", Prentice Hall.
3. L. T. Wang, C. W. Wu, and X. Wen, VLSI Test Principles and Architectures, Morgan Kaufmann, 2006, ISBN-13: 978-0-12-370597-6, ISBN-10: 0-12-370597-5.
4. System-on-a-Chip Verification-Methodology and Techniques, P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001
5. Janick Bergeron, "Writing test benches functional verification of HDL models" Kluwer Academic Publishers, New York, Boston, Dordrecht, London, Moscow, 2002.

MTVLSIS206: SEMINAR I

Weekly Practical Hours:04	Credit: 02			Tut: -
Scheme of Marking	TH: -	PR/OR: 50	IA: 50	Total: 100

The seminar shall be on the state of the art in the area of the VLSI Design Domain and of student's choice approved by an authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute.

MTVLSIP207: MINI PROJECT

Weekly Practical Hours:04	Credit: 02			Tut: -
Scheme of Marking	TH: -	PR/OR: 50	IA: 50	Total: 100

Content
The mini project shall be based on the recent trends in the industry, research and open problems from the industry and society. This may include mathematical analysis, modeling, simulation, and hardware implementation of the problem identified. The mini project shall be of the student's choice and approved by the guide. The student has to submit the report of the work carried out in the prescribed format signed by the guide and head of the department/institute.

Elective-I

MTVLSIE114 A: Image Processing & Computer Vision

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

1	To understand image fundamentals and how digital images can be processed
2	To understand image enhancement, image compression techniques and its application
3	Fundamentals of computer vision, geometrical features of images, object recognition
4	Explore application of real time image processing.

Course Outcomes:

At the end of course, students should:

CO1	Recognize the fundamental techniques of Image Processing and Computer Vision.
CO2	Interpret the basic skills of designing image compression.
CO3	Distinguish between different image compression standards.
CO4	Analyze different computer vision techniques
CO5	Analyze real time image processing system.
CO6	Explore applications of computer vision

Unit 1: Digital Image Fundamentals: A Simple Image Model, Sampling and Quantization, Relationship between Pixel, Image Formats and Image Transforms **(6hrs)**

Unit 2: Image Enhancement: Histogram processing, image subtraction, image averaging, smoothing filters, sharpening filters, enhancement in frequency and spatial domain, low pass filtering, high pass filtering. **(7hrs)**

Unit 3: Image Compression: Fundamentals, Image Compression Models, Elements of Information Theory, Error-Free Compression, Lossy Compression, Recent Image Compression Standards. **(6hrs)**

Unit 4: Real Time Image Processing: Introduction to Digital Signal Processor (TMS320CXX), Introduction to Texas Instruments Image Library, Development of a real time image processing algorithms **(7hrs)**

Unit 5: Computer Vision: Imaging Geometry, Coordinate transformation and geometric warping for image registration, Hough transforms and other simple object recognition methods, Shape correspondence and shape matching, Principal Component Analysis, Shape priors for recognition, Implementation of computer vision algorithms using Raspberry Pi. **(7hrs)**

Unit 6: Image Processing and Computer Vision Applications: Denoising of Image as pre-processing, Object recognition, Motion estimation, Object Tracking, Vision based control, vision for human computer interaction **(7hrs)**

Text Books:

1. Gonzalez, R.C., and Woods, R.E., Digital Image Processing, Dorling Kingsley (2009) 3rd Ed
2. Jain A.K., Fundamentals of Digital Image Processing, Prentice Hall (2007).
3. Sonka M., Image Processing and Machine Vision, Prentice Hall (2007) 3rd Ed.
4. D. Forsyth and J. Ponce, Computer Vision - A modern approach, Prentice Hall.

Reference Books:

1. Tekalp A.M., Digital Video Processing, Prentice Hall (1995).
2. Ghanbari M., Standard Codecs: Image Compression to Advanced Video Coding, IET Press (2003).
3. E. Trucco and A. Verri, Introductory Techniques for 3D Computer Vision, Prentice Hall.

MTVLSIE114 B: Programming Language for Embedded Systems

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

1	To understand concept of C programming
2	Understand concept of OOPs
3	Explore different scripting languages

Course Outcomes:

At the end of course, students should:

CO1	Write an embedded C application of moderate complexity.
CO2	Develop and analyze algorithms in C++.
CO3	Differentiate interpreted languages from compiled languages.
CO4	Analyze different operators in C++
CO5	Explore concept of inheritance
CO6	Explore various scripting languages

Unit 1: Embedded "C" Programming: Bitwise operations, Dynamic memory allocation, OS services. Linked stack and queue, Sparse matrices, Binary tree. Interrupt handling in C, Code

optimization issues, Embedded Software Development Cycle and Methods **(6hrs)**

Unit 2: Object Oriented Programming: Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism. **(6hrs)**

Unit 3: CPP Programming: cin, cout formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, pointer, constructors, destructors, friend function, dynamic memory allocation **(7hrs)**

Unit 4: Overloading and Inheritance: Need of operator overloading, overloading the assignment, Overloading using friends, type conversions, single inheritance, base and derived classes, friend Classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, Polymorphism, virtual functions **(7hrs)**

Unit 5: Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions. **(7hrs)**

Unit 6: Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL, Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing. **(7hrs)**

Text Books:

1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O"Reilly Publications, 6th Edition 2011
3. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005Kaufmann

Reference Books:

1. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999

MTVLSIE114 C: Mixed Signal Design

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

1	Understand basics of comparator circuits
2	Implementation of A/D and D/A converters
3	Converters performance analysis with design challenges.

Course Outcomes:

At the end of course, students should:

CO1	Apply knowledge of mathematics, science, and engineering to design CMOS analog circuits to achieve performance specifications.
CO2	Identify, formulates, and solves engineering problems in the area of mixed-signal design
CO3	Analyze different data acquisition systems
CO4	Explore data converter architecture
CO5	Analyze various analog circuit designs
CO6	Develop mixed signal based design

Unit 1: Introduction: Device Models, IC Process for Mixed Signal, Concepts of MOS Theory. Comparators: Circuit Modeling, Auto Zeroing Comparators, Differential Comparators, Regenerative Comparators, Fully Differential Comparators, Latched Comparator. **(7hrs)**

Unit 2: Data Converters: Requirements, Static and Dynamic Performance, SNR and BER, DNL, INL High Speed A/D Converter Architectures: Flash, Folding, Interpolating, pipelined High Speed D/A Converter Architectures: Nyquist-Rate D/A Converters, Thermometer Coded D/A Converters, Binary Weighted D/A Converter **(7hrs)**

Unit 3: Design: Design of multi channel low level and high level data acquisition systems using ADC/DAC, SHA and Analog multiplexers, designing of low power circuits for transducers. **(6hrs)**

Unit 4: Sigma-Delta Data Converter Architectures: Programmable Capacitor Arrays (PCA), Switched Capacitor converters, Noise Spectrum, Sigma-Delta Modulation Method, Sigma-Delta A/D and D/A Converters, Non Idealities. **(6hrs)**

Unit 5: Key Analog Circuit Design: Analog VLSI building blocks, Operational Amplifiers for converters, advanced op-amp design techniques, Voltage Comparators, Sample-and-Hold Circuits. Implementation and Design of High Performance A/D and D/A Converters: System Design, Digital Compensation, Noise, and Mismatch, Layout and Simulation Technologies for Data Converters. **(7hrs)**

Unit 6: Design Challenges: Low Voltage Design, Ultra-High Speed Design, High Accuracy Design. Advanced Topics: Multipliers, Oscillators, Mixers, Passive Filter Design, Active filter design, Switched Capacitor Filters, Frequency Scaling, Phase-Locked Loops, Device Modeling for AMS IC Design, Concept of AMS Modeling and Simulation. **(7hrs)**

Text Books:

1. Baker, R.J., Li, H.W. and Boyce, D.E., CMOS: Circuit Design, Layout and Simulation, IEEE Press (2007) 2nd ed

2. Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing,

Wiley (2002).

Reference Books:

1. Plassche, Rudy J.Van De, Integrated A-D and D-A Converters, Springer (2007), 2nd ed.

2. Jespers, P.G. A., Integrated Converters: D-A and A-D Architectures, Analysis and Simulation, Oxford University Press (2001).

MTVLSIE114 D: RF Engineering

Weekly Teaching Hours: 3 TH: 03 Tut: -

Scheme of Marking TH: 60 Tests : 20 IA: 20 Total : 100

Course Objectives:	
	This course enables the students to:
1	The objective of this course is to provide students with a comprehensive understanding of Radio Frequency (RF) engineering principles, techniques, and applications.
2	Students will learn about RF system design, transmission lines, antennas, microwave circuits, and the practical aspects of RF engineering to design, analyze, and optimize wireless communication systems.
Course Outcomes:	By the end of this course, students will be able to:
CO1	Understand the fundamental concepts of RF engineering and its importance in wireless communication systems.
CO2	Design and analyze RF systems, including RF amplifiers, oscillators, and frequency synthesizers.
CO3	Analyze and optimize the performance of transmission lines and RF networks.
CO4	Design and analyze RF antennas for various wireless applications.
CO5	Demonstrate proficiency in using RF simulation software tools.
CO6	Apply RF engineering principles to real-world communication systems and troubleshoot RF-related issues.
Syllabus Contents	
Unit 1	Introduction to RF Engineering - Overview of RF engineering and its applications in wireless communication. - Frequency bands and spectrum allocation for various wireless systems. - RF system parameters and performance metrics. Transmission Lines and Waveguides - Characterization of transmission lines: impedance, reflection coefficient, and standing waves. - Smith Chart and its applications in impedance matching. - Types of waveguides and their properties. **(6hrs)**
Unit 2	RF System Design - Design considerations for RF amplifiers, oscillators, and frequency synthesizers.

	- Noise figure and noise temperature in RF systems. - Phase-locked loops (PLL) and frequency synthesis techniques. RF Network Analysis - S-parameters and their application in RF network analysis. - Matching networks and impedance transformation. - Scattering matrices and cascade analysis. **(7hrs)**
Unit 3	Microwave Circuits and Components - Microwave passive components: couplers, splitters, and filters. - Active microwave devices: PIN diodes, GaAsFETs, and HEMTs. - Microwave integrated circuits (MIC) and monolithic microwave integrated circuits (MMIC). RF Antennas - Fundamental principles of antenna theory. - Different types of RF antennas: wire antennas, patch antennas, and array antennas. - Antenna radiation patterns and impedance matching. **(7hrs)**
Unit 4	RF Simulation Tools - Introduction to RF simulation software (e.g., ADS, CST, HFSS). - Simulating and optimizing RF circuits and antennas using software tools. - Practical lab sessions using simulation tools. **(6hrs)**
Unit 5	RF Interference and Noise - Sources of RF interference and its impact on communication systems. - Noise in RF systems: thermal noise, shot noise, and flicker noise. - Noise figure and noise factor calculations. **(7hrs)**
Unit 6	RADAR: Introduction, Classifications, Radar range equation, Modulators, Displays, Scanning andtracking, Doppler effect, Blind speeds, FMCW radars, radar antennas. **(7hrs)**
Text Books	
	1. "Microwave Engineering" by David M. Pozar, Wiley (or latest edition).
	2. "RF Microelectronics" by Behzad Razavi, Prentice Hall (or latest edition).
Reference Books	
	1. "RF Circuit Design" by Richard C. Li, Wiley (or latest edition).
	2. "Antenna Theory: Analysis and Design" by Constantine A. Balanis, Wiley (or latest edition).

MTVLSIE114 E: VLSI Signal Processing

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

1	Introduce students to the fundamentals of VLSI signal processing and expose them to examples of applications.
2	Design and optimize VLSI architectures for basic DSP algorithms.
3	Design low power signal processing applications.

Course Outcomes:

At the end of course, students should:

CO1	Able to modify the existing or new DSP architectures suitable for VLSI.
CO2	Understand the concepts of folding and unfolding algorithms and applications.
CO3	Implement fast convolution algorithms.
CO4	Able to design low power signal processing and wireless applications.
CO5	Implement digital filter
CO6	Analyze low power design approach

Unit 1: Introduction to DSP: DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms pipelining and parallel processing introduction, Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for Low Power Retiming introduction, Definitions and Properties, Solving System of inequalities, Retiming Techniques **(7hrs)**

Unit 2: Folding and Unfolding: Folding- introduction, folding transform, Register minimization Techniques, Register minimization in folded architectures, folding of multirate systems Unfolding-introduction, An algorithm for unfolding, properties of unfolding, critical Path, unfolding and retiming, applications of unfolding **(7hrs)**

Unit 3: Systolic Architecture Design: Introduction, Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix multiplication and 2D Systolic array design, Systolic design for space representations contain delays. **(6hrs)**

Unit 4: Fast Convolution: Introduction, Cook-Toom algorithm, Winogard algorithm, Iterated convolution, Cyclic convolution, Design of fast convolution algorithm by inspection. **(7hrs)**

Unit 5: Digital filter: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines. **(7hrs)**

Unit 6: Low Power Design: Scaling vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches. **(6hrs)**

Text Books:

1. Keshab K. Parhi. VLSI Digital Signal Processing Systems, Wiley-Inter Sciences

2. Kung. S.Y., H.J. While house T.Kailath, VLSI and Modern singal processing, Prentice Hall, 1985.

Reference Books:

1. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing, McGraw Hill, 1994.
2. Jose E. France, YannisTsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing' Prentice Hall, 1994.

Elective-II

MTVLSIE125 A: Parallel Processing

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	To understand concept of parallel processing.
2	Different processors and its architecture
3	Explore parallel programming architecture

Course Outcomes:

At the end of course, students should:

CO1	Identify limitations of different architectures of computer
CO2	Analysis quantitatively the performance parameters for different architectures
CO3	Investigate issues related to compilers and instruction set based on type of architectures.
CO4	Analyze multiprocessor architecture
CO5	Analyze various parallel programming techniques
CO6	Explore application area of parallel processing

Unit 1: Introduction to Parallel Processing: Overview of Parallel Processing and Pipelining, Performance analysis, Scalability. **(6hrs)**

Unit 2: Pipelining: Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining. **(7hrs)**

Unit 3: VLIW processors and Architecture: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC,MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture. **(7hrs)**

Unit 4: Multithreading: Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions. **(8hrs)**

Unit 5: Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems customizing applications on parallel processing platforms. **(8hrs)**

Unit 6: Case Study and Applications areas of parallel processing. **(4hrs)**

Text Books:

1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition

2. Kai Hwang, "Advanced Computer Architecture", TMH

3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.

Reference Books:

1. William Stallings, "Computer Organization and Architecture, Designing for performance "Prentice Hall, Sixth edition

2. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing", MGH

MTVLSIE125 B: System Design with Embedded Linux

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	To understand the embedded Linux development model
2	To be able to write and debug applications and drivers in embedded Linux.
3	To be able to understand and create Linux BSP for a hardware platform

Course Outcomes:

At the end of course, students should:

CO1	Knowledge about embedded Linux development model.
CO2	Write drivers in embedded linux environment
CO3	Understand different hardware platform
CO4	Explore flavors of embedded linux
CO5	Understand IDE, root file system with respect to linux
CO6	Analyze various toolkit for linux

Unit 1: Introduction to Embedded Linux: Embedded Linux , Vendor Independence, Time to Market,Varied Hardware Support, Open Source, Standards (POSIX®) Compliance, Embedded Linux Versus Desktop Linux, Embedded Linux Distributions, BlueCat Linux, Cadenux , Denx, Embedded Debian (Emdebian), ELinOS (SYSGO), Metrowerks ,MontaVista Linux, RTLinuxPro, TimeSys Linux. **(7hrs)**

Unit 2: Architecture of Embedded Linux: Embedded Linux Architecture, Real-Time Executive, Monolithic Kernels, Microkernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence, Boot Loader Phase, Kernel Start-Up, User Space Initialization. **(7hrs)**

Unit 3: Embedded Storages: Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules. **(6hrs)**

Unit 4: Porting Applications, Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver, Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux. **(8hrs)**

Unit 5:Building and Debugging : Kernel, Building the Kernel, Building Applications, Building the Root File System, Integrated Development Environment, Debugging Virtual Memory Problems , Kernel Debuggers, Root file system Embedded Graphics. Graphics System, Linux Desktop Graphics, Embedded Linux Graphics, Embedded Linux Graphics Driver, Windowing Environments. **(8hrs)**

Unit 6: Case study and applications: Case study of uC linux, Toolkits, and Applications. **(4hrs)**

Text Books:

1. KarimYaghmour, "Building Embededd Linux Systems", O'Reilly & Associates

2. P Raghvan, Amol Lad, Sriram Neelakandan, "Embedded Linux System Design and Development", Auerbach Publications

Reference Books:

1. Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach", Prentice Hall, 2nd Edition, 2010.

2. Derek Molloy, "Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014

MTVLSIE125 C: CAD of Digital Systems

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	To understand the fundamentals of CAD tools for modeling, design, test and verification of VLSI Systems
2	To study various phases of CAD, including simulation, physical design, test and Verification.
3	To be able to demonstrate the knowledge of computational algorithms and tools for CAD

Course Outcomes:

At the end of course, students should:

CO1	Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.
CO2	Understand various phases of CAD, including simulation, physical design, test and verification.
CO3	Explore various optimization algorithms
CO4	Analyze various simulation models
CO5	Implement simple circuit using VHDL tools
CO6	Demonstrate knowledge of tools for CAD

Unit 1: Introduction to VLSI Methodologies: Design and Fabrication of VLSI Devices, Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules Layout of Basic Devices, Fabrication Process and its Impact on Physical Design, Scaling Methods, Status of Fabrication Process, Issues related to the Fabrication Process, Future of Fabrication Process , Solutions for Interconnect Issues, Tools for Process Development. **(7hrs)**

Unit 2: VLSI design automation tools: Data Structures and Basic Algorithms, Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, graph theory and Computational complexity, tractable and intractable problems. **(6hrs)**

Unit 3: General purpose methods for combinational optimization: Partitioning- Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms , Simulated Annealing Simulated Evolution, Other Partitioning Algorithms Performance Driven Partitioning Floor planning- Chip planning , Pin Assignment , Integrated Approach, Placement- Problem Formulation , Classification of Placement Algorithms, Simulation Based Placement Algorithms , Partitioning Based Placement Algorithms , Performance Driven Placement, Routing -Global Routing, , Problem Formulation , Classification of Global Routing Algorithms,

Maze Routing Algorithms , Line-Probe Algorithms, Shortest Path Based Algorithms. Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing. **(9hrs)**

Unit 4: Simulation: Gate-level Modeling and Simulation, Switch-level Modeling and Simulation, Logic Synthesis and Verification - Introduction to Combinational Logic Synthesis , Binary-decision Diagrams, Two-level Logic Synthesis, High-level Synthesis- Hardware Models for High level Synthesis , Internal Representation of the Input Algorithm , Allocation, Assignment and Scheduling. **(7hrs)**

Unit 5: MCMs-VHDL implementation of simple circuits. **(7hrs)**

Unit 6: CAD tools and their use; Design for testability. **(4hrs)**

Text Books:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".

2. S.H. Gerez, "Algorithms for VLSI Design Automation.

Reference Books:

1. M. Sarrafzadeh and C.K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996

2. D.D Gajski et al., High Level Synthesis: Introduction to Chip and System Design, Kluwer Academic Publishers, 1992

MTVLSIE125 D: Smart Antennas

Weekly Teaching Hours: 3 TH: 03 Tut: -

Scheme of Marking TH: 60 Tests : 20 IA: 20 Total : 100

Course Objectives:	
	This course enables the students to:
1	Understand the Principles of Smart Antennas & Explain 5G Communication Systems
2	Analyze Different Types of Smart Antennas & Apply Beamforming Techniques
3	Evaluate MIMO Technology & Analyze Massive MIMO Systems
4	Implement Hybrid Beamforming & Explore Smart Antenna Applications in 5G,
5	Engage in Research and Industry Trends & Develop Practical Skills, Critically Evaluate Smart Antenna Solutions, Communicate Effectively
Course Outcomes: By the end of this course, students will be able to:	
CO1	Demonstrate a comprehensive understanding of the principles, technologies, and applications of smart antennas in the context of 5G communication systems.

CO2	Differentiate between various types of smart antennas, and understand their advantages and limitations.
CO3	Evaluate the benefits and limitations of Multiple-Input, Multiple-Output (MIMO) technology, assess its impact on 5G communication systems.
CO4	Design and implement hybrid beamforming architectures to achieve efficient and cost-effective smart antenna systems for 5G communication.
CO5	Demonstrate an awareness of the latest research trends, industry implementations, and emerging technologies related to smart antennas in 5G.
CO6	Assess the impact of smart antennas on 5G network performance metrics, such as signal-to-interference-plus-noise ratio (SINR), throughput, and coverage.
Syllabus Contents	
Unit 1	Introduction to Smart Antennas: Overview of smart antennas and their evolution in wireless communication, Advantages and challenges of smart antennas in 5G networks, Types of smart antennas: adaptive antennas, switched beam antennas, phased array antennas, etc. Antenna Fundamentals: Electromagnetic principles for antenna design, Antenna radiation patterns and gain, Antenna array configurations and their characteristics. **(7hrs)**
Unit 2	Fixed Sidelobe Canceling, Retrodirective Arrays, Beamforming, Adaptive Arrays, Butler Matrix, Spatial Filtering with Beamformers, Switched Beam Systems, Multiple Fixed Beam System. Uplink Processing. **(6hrs)**
Unit 3	Diversity Techniques, Angle Diversity, Maximum Ratio Combining, Adaptive Beamforming, Fixed Multiple Beams versus Adaptive Beamforming, Downlink Processing. **(7hrs)**
Unit 4	Fundamentals of Matrix Algebra, Array Correlation Matrix, AOA Estimation Methods: Bartlett AOA Estimate, Capon AOA Estimate, Linear Prediction AOA Estimate, Maximum Entropy AOA Estimate, Pisarenko Harmonic Decomposition AOA Estimate, Min-Norm AOA Estimate, MUSIC AOA Estimate, ESPRIT AOA Estimate. **(7hrs)**
Unit 5	Introduction, Multiple-Antenna MS Design, RAKE Receiver Size, Mutual Coupling Effects, Dual-Antenna Performance Improvements, Downlink Capacity Gains. **(7hrs)**
Unit 6	Principles of MIMO systems: SISO, SIMO, MISO,MIMO, Hybrid antenna array for mmWave massive MIMO: Massive Hybrid Array Architectures, Hardware Design for Analog Subarray. Current research and industry trends in smart antennas for 5G. **(7hrs)**
Text Books	
1	Smart Antennas for Wireless Communications: With MATLAB by Frank Gross, Publisher: McGraw-Hill Education ISBN-13: 978-0070242843, ISBN-10: 0070242849
2	Smart Antennas for Wireless Communications: IS-95 and Third Generation CDMA Applications by Thomas T. K. Tan, Publisher: Prentice Hall, ISBN-13: 978-0130862252, ISBN-10: 0130862252
3	Smart Antennas for Next Generation Wireless Systems, by Y. Jay Guo and Iain Colling Artech House, ISBN-13: 978-1630818124; ISBN-10: 1630818126

MTVLSIE125 E: ASIC Design

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	To be an entry-level industrial standard ASIC or FPGA designer.
2	Understanding of issues and tools related to ASIC/FPGA design and implementation.
3	Understanding of basics of System on Chip and Platform based design

Course Outcomes:

CO1	Able to demonstrate VLSI tool-flow and appreciate FPGA and CPLD architectures
CO2	Able to understand the issues involved in ASIC design, including technology choice, design management and tool-flow.
CO3	Able to understand the algorithms used for ASIC construction
CO4	To understand about STA, LEC, DRC, LVS, DFM
CO5	Able to understand Semicustom Design Flow and Tool used – from RTL to GDS and Logical to Physical Implementation
CO6	Able to understand the basics of System on Chip and on chip communication architectures appreciate high performance algorithms for ASICs

Unit 1: Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules, Programmable ASICs, Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Advanced FPGAs and CPLDs and Soft-core processors. **(7hrs)**

Unit 2: ASIC physical design issues, System Partitioning, Floor planning and Placement. Algorithms: K-L, FM, Simulated annealing algorithms. Full Custom Design: Basics, Needs & Applications. Schematic and layout basics, Full Custom Design Flow. **(7hrs)**

Unit 3: Semicustom Approach: Synthesis (RTL to GATE netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floor plan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, Timing Optimization, GDS generation. **(7hrs)**

Unit 4: Extraction, Logical equivalence and STA: Parasitic Extraction Flow, STA: Timing Flow, LEC: Introduction, flow and Tools used. Physical Verification: Introduction, DRC, LVS and basics of DFM. **(7hrs)**

Unit 5: System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. **(6hrs)**

Unit 6: High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC. **(6hrs)**

Text Books:

1. Sudeep Pasricha and Nikil Dutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008
2. M.J.S. Smith : Application Specific Integrated Circuits, Pearson, 2003
3. N. Jha & S.D. Gupta, "Testing of Digital Systems", Cambridge, 2003

Reference Books:

1. Jan. M.Rabaey et al, Digital Integrated Circuit Design Perspective (2/e), PHI 2003
2. David A.Hodges, Analysis and Design ofDigital Integrated Circuits (3/e), MGH 200

Elective-III

MTVLSIE233 A: Memory Technologies

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	To know the RAM technologies, architecture and applications
2	To know the circuit design concepts of Non-volatile memories
3	To understand the Memory package density technologies

Course Outcomes:

CO1	Select architecture and design semiconductor memory circuits and subsystems
CO2	Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
CO3	Know, how of the state-of-the-art memory chip design
CO4	Explore nonvolatile memories
CO5	Analyze high performance memories and its power dissipation
CO6	Analyze issues of low voltage memory design

Unit 1: Introduction to Memory Chip Design: Basics of Semiconductor Memory, Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Architectures of memory cell: SRAM Cell, DRAM Cell Trends in Non-Volatile Memory Design and Technology, Ferroelectric memory, Basic

Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology. **(7hrs)**

Unit 2: Basics of RAM Design and Technology: Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law. **(6hrs)**

Unit 3: DRAM Circuits: High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, Write and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal-to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources. **(7hrs)**

Unit 4: Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories. **(6hrs)**

Unit 5: High-Performance Subsystem Memories: Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories. Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits. **(7hrs)**

Unit 6: Ultra-Low-Voltage Memory Circuits: Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Sub threshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits. **(7hrs)**

Text Books:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
2. Kiyoo Itoh, "VLSI memory chip design", Springer International Ed.

Reference Books:

1. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability, PHI
2. Adams, R. D., High performance Memory Testing: Design Principles, Fault Modeling and Self-Test, Springer (2002)
3. Prince, B., Semiconductor Memories: A handbook of Design, Manufacture and Application, John Wiley (1996) 2nd ed.

MTVLSIE233 B: System On-Chip Design

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	Learn SOC design processes
2	To understand ASIC design flow
3	Understand test optimization with system integration issues

Course Outcomes:

At the end of course, students should:

CO1	Acquire knowledge about Top-down SoC design flow.
CO2	Understand the ASIC Design flow and EDA tools
CO3	Identify and formulate a given problem in the framework of SoC based design approach
CO4	Design SoC based system for engineering applications
CO5	Understand the designing communication Networks.
CO6	Realize impact of SoC on electronic design philosophy and Macro-electronics

Unit 1: ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts. **(6hrs)**

Unit 2: NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors. **(7hrs)**

Unit 3: Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues. **(7hrs)**

Unit 4: Low power SoC design: Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification. **(7hrs)**

Unit 5: Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization

constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs. **(7hrs)**

Unit 6: SOC Test Optimizations: Design methodologies for SoC, Noise and signal integrity analysis, System Integration issues for SoC, SoC Test Scheduling and Test Integration, SoC Test Resource partition. **(6hrs)**

Text Books:

1. Wolf, W., Modern VLSI Design: System-on-chip Design, Prentice Hall (2002) 3rd ed.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
3. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008

Reference Books:

1. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center,2000
2. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley

MTVLSIE233 C: Low Power VLSI Design

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	To understand the causes of the power dissipation in digital ICs
2	Quantitative analysis of power dissipation in VLSI circuits
3	Exploring the low power circuits and architectures for VLSI system.

Course Outcomes:

At the end of course, students should:

CO1	Understand the need for low power in VLSI.
CO2	Understand various dissipation types in CMOS.
CO3	Estimate and analyze the power dissipation in VLSI circuits
CO4	Understand the probabilistic power techniques.
CO5	Analyze memory design techniques
CO6	Demonstrate circuit simulation of memory design

Unit 1: Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices. **(7hrs)**

Unit 2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches. **(6hrs)**

Unit 3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. Tolerable skew, chip & package co-design of clock network. **(7hrs)**

Unit 4: Logic Synthesis for Low Power estimation techniques: Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers. **(7hrs)**

Unit 5: Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits. Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power. **(7hrs)**

Unit 6: Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, Monte Carlo simulation. **(6hrs)**

Text Books:

1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc.,2000.

Reference Books:

1. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design",Kluwer,1995
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

MTVLSIE233 D: Computer Networks

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	Understand computer networks concepts and design.
2	To understand computer network architectures, protocols, and interfaces
3	To understand the OSI reference model and the Internet architecture network applications.

Course Outcomes:

At the end of course, students should:

CO1	Implement Network Layer Protocols.
CO2	Configure IPvX network.
CO3	Choose routing protocol in given network.

CO4	Implement different transport layer protocols
CO5	Implement different network architectures.
CO6	Explore various network security algorithms.

Unit 1: Review of computer networking: ISO-OSI reference model, Point to point Protocol, ARQ techniques, Data network switching techniques. **(6hrs)**

Unit 2: TCP/IP: TCP/IP architecture, TCP Segments, TCP flow control, IPv4 versus IPv6, UDP, Fragmentation, ARP & RARP , ICMP,IGMP, DHCP, Mobile IP, Unicast and Multicast Routing protocols. **(7hrs)**

Unit 3: Network management: Delay models in data networks, Performance measures & architectural Issues, Queuing Model (M/M/1, M/M/C, and M/G/1), Network management and congestion control algorithm. **(7hrs)**

Unit 4: ATM Networks: Need for ATM, B-ISDN reference model, ATM Layers, ATM adaptation Layers, ATM Signaling, PNNI routing, QoS in ATM. **(7hrs)**

Unit 5: Advance Network Architecture: Overlay model, MPLS, Integrated services, Differentiated services, RSVP. **(7hrs)**

Unit 6: Network Security: Ciphers, DES, public key cryptography, RSA algorithm, Digital water marking, Attack and counter measure. **(6hrs)**

Text Books:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience

2. Kiyoo Itoh, "VLSI memory chip design", Springer International Ed.

Reference Books:

4. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability, PHI
5. Adams, R. D., High performance Memory Testing: Design Principles, Fault Modeling and Self-Test, Springer (2002)
6. Prince, B., Semiconductor Memories: A handbook of Design, Manufacture and Application, John Wiley (1996) 2nd ed.

MTVLSIE233 E: Real Time Embedded System Design

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	Introduction to embedded system architecture & its software.
2	Enabling students to design an Embedded system using various methodologies.
3	Preparing students to build process for an Embedded system.

Course Outcomes:

At the end of course, students should:

CO1	Comprehend Embedded Processor and its software
CO2	Design an Embedded system with different modeling techniques
CO3	Build a process for an Embedded system
CO4	Design an Embedded system using processors, memory I/O devices and communication networks.
CO5	Incorporate operating system in an Embedded system.
CO6	Comprehend the operation of multitasking in an Embedded System and implementation

Unit 1: Embedded System hardware : Embedded systems overview, Hardware components like microcontroller, GPP, ASSP, AISP, SOC, Details of 32 bit ARM7 core based SoC architecture, Organization, analog, digital & high speed I/O for embedded systems, interfacing SRAM, DRAM, flash memories with microcontroller, memory management. **(6hrs)**

Unit 2: Embedded System Software : Techniques of writing efficient C code for microcontroller C data types for ARM, Signed & unsigned data types, limitation of char & char & data types, storage class – static & extern, volatile keyword, operation on bits, functions, ARM / Thumb procedural call standard, pointers & arrays, conditional statements – if else, switch, structure, conditional loops – for & while, preprocessing, compiling, cross compiling, compiler driver, startup code and board support packages, calling assembly routines in C, interrupt handling in C, interrupt latency. **(7hrs)**

Unit 3: ARM Philips NXP LPC2148 Microcontroller: Programming & Interfacing: Programming on – chip components like ADC, UART, Timers, External Interrupts and interfacing external peripherals like keyboard, LCD, Stepper motor. **(7hrs)**

Unit 4: Uniprocessor Real Time Operating Systems – I: Real time systems, goals and services, tasks and its states, task assignment & scheduling, Task Control Blocks, Context & Context Switching, ISRs, Security Issues, inter- task communication, semaphore. **(7hrs)**

Unit 5: Uniprocessor Real Time Operating Systems – II: Task Scheduling models, scheduling algorithms – rate monotonic and earliest deadline first, priority inheritance protocol, priority ceiling protocol, real time

operating system features, features of micro COS – II RTOS. **(7hrs)**

Unit 6: Embedded System Architecture & Design: Architecture styles, implementation aspects, estimation modeling, embedded system architecture, validation and debugging of embedded systems. **(6hrs)**

Text Books:

1. "Embedded Systems", Rajkamal, 2nd Edi.,Tata Mc-Graw Hill.
2. "Embedded Real-time System Programming", Iyer & Gupta, Tata Mc-Graw Hill.

Reference Books:

1. "ARM System on Chip Architecture", Furber, 2nd Edi Pearson India. Adams, R. D., High performance Memory Testing: Design Principles, Fault Modeling and Self-Test, Springer (2002)
2. "Introduction to Embedded System", K. V. Shibu, MGH.
3. "Philips NXP LPC 2148" user manual
4. "Scheduling in Real Time Systems", Cottet, Delacroix & Mammeri, John Wiley & Son.
5. "Real Time Systems", Rajib Mall, Pearson, India.

Elective-IV

MTVLSIE244 A: Network Security and Cryptography

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests:20	IA:20	Total:100

Course Objectives:	
	This course enables the students:
1	To imbibe good foundation of network security in students for implementation of new network security algorithms.
2	To understand different network models and the protocols used in each layer.
3.	To acquire detailed approach of encryption decryption for the data to transmit
4.	To understand the role of network security as a tool for protection of different network entities
5.	To be able to accurately apply security algorithms to real world security issues.
6.	To ensure windows and web browser security through implementation of various encryption standards.
Course Outcomes: By the end of this course, students will be able to:	
CO1	Analyze attacks on computers and computer security.
CO2	Demonstrate knowledge of cryptography techniques
CO3	Illustrate various Symmetric and Asymmetric keys for Ciphers
CO4	Evaluate different Message Authentication Algorithms and Hash Functions.
CO5	Get acquainted with various aspects of E-Mail Security
CO6	Assimilate various aspects of Web Security
Syllabus Contents	
Unit 1	Introduction to Cryptography and Network Security - Overview of cryptography and its historical context.

	- Introduction, The need for security, Security approaches, Principles of security, Types of Security attacks, Security services, Security Mechanisms, A model for Network Security. **(7hrs)**
Unit 2	Introduction, plain text and cipher text, substitution techniques, transposition techniques, encryption and decryption, symmetric and asymmetric key cryptography, stenography, key range and key size, possible types of attacks. **(7hrs)**
Unit 3	Block Cipher principles & Algorithms (DES, AES, Blowfish), Differential and Linear Crypt analysis, Block cipher modes of operation, Stream ciphers, RC4, Location and placement of encryption function, Key distribution, Asymmetric key Ciphers, Principles of public key crypto systems, Algorithms (RSA, Diffie Hellman, ECC). **(7hrs)**
Unit 4	Authentication requirements, Functions, Message authentication codes, Hash Functions, Secure hash algorithm, HMAC, CMAC, Digital signatures, knapsack algorithm, Authentication Applications such as Kerberos, X.509 Authentication Service, Public – Key Infrastructure, Biometric Authentication. **(7hrs)**
Unit 5	Pretty Good Privacy, S/MIME, IP security overview, IP Security architecture, Authentication Header, Encapsulating , Security payload, Combining security associations, Key management. **(6hrs)**
Unit 6	Web security considerations, Secure Socket Layer and Transport Layer Security, Secure electronic transaction, Intruders, Intrusion detection, password management, virus and related threats, Countermeasures, Firewall design principles, types of firewalls, SET Protocol. Emerging Trends in Cryptography and Network Security: - Case study : Blockchain technology and its security implications. **(6hrs)**
Text Books	
	1. William Stallings, "Cryptography and Network Security" ,Pearson Education, 4 th Edition 2. Atul Kahate, "Cryptography and Network Security", McGraw Hill, 3rd Edition. 3. C K Shymala, N Harini, Dr. T R Padmanabhan, "Cryptography and Network Security", Wiley India,1st Edition
Reference Books	
	1. Forouzan Mukhopadhyay, "Cryptography and Network Security", Mc Graw Hill, 2 ndEdition. 2. Mark Stamp, "Information Security, Principles and Practice", Wiley India, 2nd Edition. 3. W.M. Arthur Conklin, Greg White, "Principles of Computer Security", TMH, 4 th Edition. 4. Neal Krawetz, "Introduction to Network Security", CENGAGE Learning Distributor, 1st Edition. 5. Bernard Menezes, "Network Security and Cryptography", CENGAGE Learning Distributor, 1st 2. Edition

MTVLSIE244 B: Physical Design Automation

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	Understand the concepts of Physical Design Process such as partitioning, Floorplanning, Placement and Routing
2	Discuss the concepts of design optimization algorithms and their application to physical design automation.
3	Understand the concepts of simulation and synthesis in VLSI Design Automation

Course Outcomes:

At the end of course, students should:

CO1	Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology
CO2	Adapt the design algorithms to meet the critical design parameters.
CO3	Identify layout optimization techniques and map them to the algorithms
CO4	Explore various algorithms for design automation
CO5	Understand planning and routing
CO6	Develop proto-type EDA tool and test its efficacy

Unit 1: Introduction: VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost. **(7hrs)**

Unit 2: Algorithms: Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms. **(7hrs)**

Unit 3: Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations. **(6hrs)**

Unit 4: Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum colouring, maximum k-independent set algorithm, algorithms for circle graphs. **(7hrs)**

Unit 5: Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms. **(7hrs)**

Unit 6: VLSI CAD tools: Automation, use of VLSI CAD tools, Algorithmic Graph Theory, Computational Complexity and ROBDD; Partitioning and Placement: KL algorithm, FM algorithm, Group-migration algorithm, Simulated Annealing and Evolution. **(6hrs)**

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

Reference Books:

1. S.M. Sait , H. Youssef, "VLSI Physical Design Automation", World scientific, 1999
2. M.Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1999

MTVLSIE244 C: Reconfigurable Computing

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:	
	This course enables the students to:
1	The objective of this course is to provide students with a comprehensive understanding of reconfigurable computing concepts, architectures, and design methodologies.
2	The course aims to equip students with the knowledge and skills required to design, implement, and optimize reconfigurable hardware systems using Field-Programmable Gate Arrays (FPGAs) and related technologies.
Course Outcomes: By the end of this course, students will be able to:	
CO1	Understand the fundamental principles and concepts of reconfigurable computing.
CO2	Analyze and evaluate different types of reconfigurable hardware architectures.
CO3	Design and implement reconfigurable systems using FPGAs.
CO4	Optimize and customize hardware designs for specific applications.
CO5	Apply their skills to solve real-world challenges in reconfigurable computing.
CO6	Stay updated with emerging trends and advancements in reconfigurable computing technologies.
Syllabus Contents	
Unit 1	Introduction to Reconfigurable Computing - Basics of reconfigurable computing: definition and applications. - Evolution of reconfigurable hardware technologies. - Challenges and advantages of reconfigurable computing. Field-Programmable Gate Arrays (FPGAs) - FPGA architecture and components. - FPGA programming languages: VHDL. - FPGA design flow and development tools. **(7hrs)**
Unit 2	Reconfigurable Hardware Design Techniques - Sequential and combinational logic design on FPGAs. - Design optimization and resource management. - Timing constraints and performance analysis.

	Hardware Description Languages (HDLs) - Introduction to VHDL. - HDL-based design methodologies. - Synthesis and simulation tools for HDLs. **(7hrs)**
Unit 3	High-Level Synthesis (HLS) - Introduction to HLS and its advantages. - C-based design and optimization. - Mapping C using code to hardware HLS tools. Reconfigurable Computing Architectures - Configurable logic blocks and interconnects. - Partial and dynamic reconfiguration techniques. - Coarse-grained and fine-grained reconfigurable architectures. **(7hrs)**
Unit 4	Reconfigurable Computing Applications - Hardware acceleration for compute-intensive tasks. - Digital signal processing on FPGAs. - Reconfigurable computing in cryptography, networking, and image processing. **(7hrs)**
Unit 5	Reconfigurable Systems for Machine Learning - FPGA-based accelerators for neural networks. - Hardware-software co-design for AI applications. - FPGA-based inference engines. **(6hrs)**
Unit 6	Emerging Trends in Reconfigurable Computing - Reconfigurable computing for edge and IoT applications. - Quantum reconfigurable computing. - Reconfigurable computing in the context of advanced communication technologies. **(6hrs)**
Text Books	
	1. "Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation" by Scott Hauck and André DeHon, Morgan Kaufmann (or latest edition).
	2. "Field-Programmable Gate Arrays" by Stephen Brown and Jonathan Rose, Springer (or latest edition).
Reference Books	
	1. "FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version" by Pong P. Chu, Wiley (or latest edition).
	2. "Digital Design and Computer Architecture" by David Harris and Sarah Harris, Morgan Kaufmann (or latest edition).

MTVLSIE244 D: VLSI Sub-system Design

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	Understand data processing elements with various architecture design
2	Acquire PLA design concepts
3	To understand memory design with its clock issues.

Course Outcomes:

At the end of course, students should:

CO1	Acquire knowledge to Design of Data Processing Elements.
CO2	Design of Control Part of digital logic circuit.
CO3	Understand control part of VLSI subsystem
CO4	Acquire knowledge about Structuring of Logic Design.
CO5	Understand architecture of memory
CO6	Identify Clocking Issues in digital system design

Unit 1: Introduction: Review of Transistor, Inverter Analysis, CMOS Process and Masking Sequence, Layer Properties and Parasitic Estimation. VLSI Design Flow, Design Methodologies, Abstraction Levels. **(7hrs)**

Unit 2: Design of Data Processing Elements: Adder Architectures, Multiplier Architectures, Counter Architectures, ALU Architectures, Design of Storage Elements: Latches, Flip-Flops, Registers, Register Files. **(7hrs)**

Unit 3: Design of Control Part: Moore and Mealy Machines, PLA Based Implementation, Random Logic Implementation, Micro-programmed Implementation. **(6hrs)**

Unit 4: Structuring of Logic Design: PLA Design, PLA Architectures, Gates Array Cell Design, Concept of Standard Cell Based Design, Cell Library Design. **(7hrs)**

Unit 5: Memory Design: SRAM cell, Various DRAM cells, RAM Architectures, Address Decoding, Read/Write Circuitry, Sense Amplifier and their Design, ROM Design. **(7hrs)**

Unit 6: Clocking Issues: Clocking Strategies, Clock Skew, Clock Distribution and Routing, Clock Buffering, Clock Domains, Gated Clock, Clock Tree. Synchronization Failure and Meta-stability. **(6hrs)**

Text Books:

1. Weste, N.H.E. and Eshragian, K., Principles of CMOS VLSI Design – A Systems Prespective, Addison Wesley (1994) 3rd ed.
2. Rabaey, J.M., Chandrakasan, A., and Nikolic, B., Digital Integrated Circuits – A Design Perspective, Pearson Education (2008) 3rd ed

Reference Books:

1. Wolf, W., Modern VLSI Design, Prentice Hall (2008) 3rd ed.
2. Uyemura, J.P., Circuit design for CMOS VLSI, Springer (2005) 2nd ed.
3. Mead, C. and Conway, L., Introduction to VLSI Systems, B.S. Publisher (1980) 2nd ed

MTVLSIE244 E: Fault Tolerant Digital System Design

Weekly Teaching Hours	TH:03			Tut: -
Scheme of Marking	TH:60	Tests:20	IA:20	Total:100

Course Objectives:

1	Understand basics of fault and error models in VLSI arithmetic
2	Understand fault tolerance strategies, detection and correction techniques
3	To understand applications of arithmetic units and systems.

Course Outcomes:

At the end of course, students should:

CO1	Acquire knowledge about fault tolerance in arithmetic circuits
CO2	Learn about Fault diagnosis, Fault tolerance measurement.
CO3	Acquire knowledge about Fault tolerance strategies
CO4	Enhance capabilities about applications of fault tolerant designs in arithmetic units and systems.
CO5	Acquire knowledge about IEEE test access methods
CO6	Acquire knowledge on Software reliability models, and methods.

Unit 1: Fault Tolerant Design: Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits. Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. **(7hrs)**

Unit 2: Self Checking circuits & Fail safe Design: Self Checking Circuits: Basic concepts, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code. Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. **(6hrs)**

Unit 3: Design for Testability: Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs. Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs. **(7hrs)**

Unit 4: Logic Built-in-self-test: BIST Basics-Memory-based BIST,BIST effectiveness, BIST

types, Designing a BIST, Test Pattern Generation-Engaging, BIST architectures-BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self – testing using MISR and SRSG, Concurrent BIST, BILBO. **(7hrs)**

Unit 5: Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. **(6hrs)**

Unit 6: Applications to arithmetic units and systems: convolves, inner product units, FFT units neural networks, Application levels: unit, processing element, subsystem, system. Cost/benefit analysis Fault- tolerant transaction processing systems; Fault-tolerant Networks; Redundant disks (RAID). Software reliability models, Software fault-tolerance methods: N-version programming, recovery blocks, rollback and recovery. Architecture and design of fault – tolerant computer systems using protective redundancy. **(7hrs)**

Text Books:

1. Parag K. Lala, "Fault Tolerant & Fault Testable Hardware Design", 1984, PH
2. Zainalabedin Navabi, "Digital System Test and Testable Design using HDL models and Architectures", Springer International Edition

Reference Books:

1. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, "Digital Systems Testing and Testable Design", Jaico Books
2. Bushnell & Vishwani D. Agarwal, "Essentials of Electronic Testing", Springer.

Elective-V (Open Elective)

MTVLSIE255 A: Artificial Intelligence & Machine Learning

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:	
1	The objective of this course is to provide students with a comprehensive understanding of artificial intelligence (AI) and machine learning (ML) concepts, techniques, and applications.
2	The course aims to equip students with the knowledge and skills required to design, implement, and apply AI and ML algorithms in communication technologies and other domains.
Course Outcomes:	
CO1	Understand the fundamental principles of artificial intelligence and machine learning.
CO2	Analyze and evaluate different AI and ML algorithms and models.
CO3	Design and implement AI and ML solutions for real-world problems.
CO4	Apply AI and ML techniques to optimize and enhance communication systems.
CO5	Utilize their skills to develop AI-driven applications in various domains.
CO6	Stay updated with emerging trends and advancements in AI and machine learning technologies.
Syllabus Contents	
Unit 1	Introduction to Artificial Intelligence - Basics of artificial intelligence: definition, history, and applications. - Comparison between AI and traditional computing approaches. - Ethical considerations in AI. Machine Learning Fundamentals - Introduction to machine learning concepts. - Types of machine learning: supervised, unsupervised, reinforcement learning. - Machine learning process: data preprocessing, training, evaluation, and deployment. **(7hrs)**
Unit 2	Supervised Learning Algorithms - Linear regression. - Logistic regression. - k-Nearest Neighbors (k-NN). - Support Vector Machines (SVM). Unsupervised Learning Algorithms - K-Means clustering. - Hierarchical clustering. - Principal Component Analysis (PCA). **(7hrs)**
Unit 3	Neural Networks and Deep Learning - Basics of artificial neural networks (ANN). - Convolutional Neural Networks (CNN). - Recurrent Neural Networks (RNN).

	- Introduction to deep learning frameworks. Reinforcement Learning - Introduction to reinforcement learning. - Markov decision processes and Q-learning. - Applications of reinforcement learning in communication technologies. **(7hrs)**
Unit 4	Natural Language Processing (NLP) - Basics of NLP: tokenization, part-of-speech tagging, sentiment analysis. - Introduction to word embeddings. - Text generation and language models. **(7hrs)**
Unit 5	AI and ML in Communication Technologies - AI-driven network management and optimization. - ML-based channel estimation and equalization. - AI for spectrum sensing and allocation. **(7hrs)**
Unit 6	Emerging Trends in AI and Machine Learning - AI in edge computing and IoT. - Explainable AI and interpretability. - AI ethics and bias considerations. **(5hrs)**
Text Books	
	1. "Pattern Recognition and Machine Learning" by Christopher M. Bishop, Springer (or latest edition).
	2. "Deep Learning" by Ian Goodfellow, Yoshua Bengio, and Aaron Courville, MIT Press (or latest edition).
Reference Books	
	1. "Artificial Intelligence: A Modern Approach" by Stuart Russell and Peter Norvig, Pearson (or latest edition).
	2. "Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow" by Aurélien Géron, O'Reilly Media (or latest edition).

MTVLSIE255 B: Operations Research

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:	
1	The objective of this course is to provide students with a comprehensive understanding of operations research principles, methodologies, and techniques.
2	The course aims to equip students with the knowledge and skills required to analyze complex engineering problems, make informed decisions, and optimize processes in communication technologies and related domains.
Course Outcomes:	
CO1	Understand the fundamental principles of operations research.
CO2	Apply mathematical models and techniques to solve engineering optimization problems.
CO3	Analyze and evaluate different operations research methodologies.
CO4	Design and implement optimization solutions for real-world problems.
CO5	Utilize their skills to improve decision-making and resource allocation in communication systems.
CO6	Stay updated with emerging trends and advancements in operations research.

Syllabus Contents	
Unit 1	Introduction to Operations Research - Basics of operations research: definition, history, and applications. - Scope and limitations of operations research. - Phases of the operations research process. Linear Programming - Formulation of linear programming problems. - Graphical solution and simplex method. - Duality and sensitivity analysis. **(7hrs)**
Unit 2	Integer and Mixed-Integer Programming - Integer programming models and applications. - Branch-and-bound algorithm for solving integer programming problems. - Cutting-plane methods. Network Optimization - Shortest path and minimum spanning tree problems. - Max flow-min cut theorem and applications. - Transportation and assignment problems. **(7hrs)**
Unit 3	Nonlinear Optimization - Unconstrained optimization techniques: gradient descent, Newton's method. - Constrained optimization: Karush-Kuhn-Tucker conditions. - Applications of nonlinear optimization in engineering. Dynamic Programming - Principles of dynamic programming. - Forward and backward recursion methods. - Applications in resource allocation and project scheduling. **(7hrs)**
Unit 4	Queuing Theory - Basics of queuing systems and models. - M/M/1 and M/M/c queuing models. - Applications of queuing theory in communication networks. **(7hrs)**
Unit 5	Decision Analysis - Decision-making under uncertainty. - Decision trees and expected value of perfect information. - Sensitivity analysis and risk assessment. **(6hrs)**
Unit 6	Emerging Trends in Operations Research - Operations research in supply chain management and logistics. - Data-driven optimization and machine learning in operations research. - Operations research in smart cities and sustainable technologies. **(6hrs)**
Text Books	
	1. "Introduction to Operations Research" by Frederick S. Hillier and Gerald J. Lieberman, McGraw-Hill (or latest edition).
	2. "Operations Research: Applications and Algorithms" by Wayne L. Winston, Cengage Learning (or latest edition).
Reference Books	
	1. "Operations Research: An Introduction" by Hamdy A. Taha, Pearson (or latest edition).
	2. "Network Flows: Theory, Algorithms, and Applications" by Ravindra K. Ahuja, Thomas L. Magnanti, and James B. Orlin, Prentice Hall (or latest edition).

MTVLSIE255 C: Business Analytics

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:	
1	The objective of this course is to provide students with a comprehensive understanding of business analytics principles, methodologies, and techniques.
2	The course aims to equip students with the knowledge and skills required to analyze and interpret data, make data-driven decisions, and apply analytical techniques in communication technologies and related domains.
Course Outcomes:	
CO1	Understand the fundamental principles of business analytics.
CO2	Apply data visualization and statistical techniques to analyze and interpret data.
CO3	Evaluate and select appropriate analytical tools for various business scenarios.
CO4	Design and implement data-driven solutions to solve real-world problems.
CO5	Utilize their skills to optimize processes and enhance decision-making in communication systems.
CO6	Stay updated with emerging trends and advancements in business analytics.
Syllabus Contents	
Unit 1	Introduction to Business Analytics - Basics of business analytics: definition, importance, and applications. - Role of data in decision-making and business strategies. - Ethical considerations in business analytics. Data Exploration and Visualization - Data preprocessing and cleaning. - Exploratory data analysis. - Data visualization techniques using tools like Tableau, Power BI, etc. **(7hrs)**
Unit 2	Descriptive and Inferential Statistics - Measures of central tendency and dispersion. - Hypothesis testing and confidence intervals. - Analysis of variance (ANOVA) and regression analysis. Predictive Analytics - Regression analysis for prediction. - Time series analysis and forecasting. - Machine learning algorithms for predictive modeling. **(7hrs)**
Unit 3	Prescriptive Analytics - Introduction to optimization and linear programming. - Decision-making under uncertainty using decision trees and Monte Carlo simulation. - A/B testing and experimental design. Text Analytics and Natural Language Processing (NLP) - Basics of text analytics and sentiment analysis. - Introduction to NLP techniques. - Applications of NLP in business insights. **(7hrs)**

Unit 4	Data Mining and Machine Learning - Clustering and classification techniques. - Feature selection and dimensionality reduction. - Introduction to machine learning algorithms. **(7hrs)**
Unit 5	Business Analytics in Communication Technologies - Analytics-driven network performance optimization. - Customer churn prediction and management. - Data-driven resource allocation in communication systems. **(6hrs)**
Unit 6	Emerging Trends in Business Analytics - Big data analytics and real-time insights. - Ethical considerations in data-driven decision-making. - Business analytics in the context of emerging technologies. **(6hrs)**
Text Books	
	1. "Business Analytics" by Ramesh Sharda, Dursun Delen, Efraim Turban, Pearson (or latest edition).
	2. "Data Science for Business" by Foster Provost and Tom Fawcett, O'Reilly Media (or latest edition).
Reference Books	
	1. "Practical Business Analytics Using SAS: A Hands-On Guide" by Venkat Reddy Konasani, Apress (or latest edition).
	2. "Analytics in a Big Data World: The Essential Guide to Data Science and its Applications" by Bart Baesens, McGraw-Hill (or latest edition).

MTVLSIE255 D: Composite Materials

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

1	Understand characteristics of Composite materials
2	To understand manufacturing technique of composites

Course Outcomes:

At the end of course, students should:

CO1	Demonstrate knowledge of composite materials
CO2	Ability to display preparation of molding compounds
CO3	Explore various metal diffusion techniques
CO4	Demonstrate methods of manufacturing molding compounds
CO5	Analyze stress and strain of material
CO6	Able to select proper material

Unit 1: Introduction: Definition, Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance. **(7hrs)**

Unit 2: Reinforcements: Preparation-layup, curing, properties and applications of glass fibers,

carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. isostrain and isostress conditions. **(8hrs)**

Unit 3: Manufacturing of Metal Matrix Composites: Casting, Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications. **(8hrs)**

Unit 4: Manufacturing of Polymer Matrix Composites: Preparation of molding compounds and prepregs, hand layup method – Autoclave method – Filament winding method – Compression molding – Reaction injection molding. Properties and applications. **(7hrs)**

Unit 5: Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations. **(7hrs)**

Unit 6: Application and case studies of different composite materials **(3hrs)**

Text Books:

1. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.

2. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.

Reference Books:

1. Composite Materials Science and Applications – Deborah D.L.Chung.

2. Composite Materials – K.K.Chawla

MTVLSIE255 E: Industrial Safety

Weekly Teaching Hours	TH: 03			Tut: -
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:	
1	The objective of this course is to provide students with a comprehensive understanding of industrial safety principles, regulations, risk management, and best practices within the context of advanced communication technologies.
2	Students will learn how to identify, assess, and mitigate potential safety hazards in technology-driven industrial environments, ensuring the well-being of employees, assets, and the surrounding environment.
Course Outcomes:	
CO1	Understand the importance of industrial safety in the context of advanced communication technologies.

CO2	Identify potential safety hazards associated with communication technology equipment and systems.
CO3	Apply risk assessment techniques to evaluate and prioritize safety risks.
CO4	Design safety protocols and measures for technology-driven industrial processes.
CO5	Comply with relevant safety regulations and standards in communication technology environments.
CO6	Develop contingency plans for emergencies and incidents.
Syllabus Contents	
Unit 1	Introduction to Industrial Safety - Importance of industrial safety in technology-intensive industries - Historical accidents and their impacts - Regulatory frameworks and standards Hazard Identification and Risk Assessment - Common hazards in communication technology environments - Risk assessment methodologies - Quantitative and qualitative risk assessment techniques. **(7hrs)**
Unit 2	Safety in Communication Technology Infrastructure - Safety considerations in data centers and network facilities - Electrical safety for advanced communication equipment - Fire prevention and control measures. **(7hrs)**
Unit 3	Human Factors and Ergonomics - Understanding human error and its role in accidents - Designing user-friendly and safe workspaces - Managing fatigue and stress in technology-intensive roles. **(7hrs)**
Unit 4	Emergency Planning and Incident Response - Developing emergency response plans - Evacuation procedures and protocols - Crisis communication strategies. **(7hrs)**
Unit 5	Compliance and Regulations - Occupational Safety and Health Administration (OSHA) regulations - International safety standards for communication technologies - Ensuring compliance in a rapidly evolving technological landscape. **(6hrs)**
Unit 6	Compliance and Regulations - Occupational Safety and Health Administration (OSHA) regulations - International safety standards for communication technologies - Ensuring compliance in a rapidly evolving technological landscape Case Studies and Best Practices - Analyzing past industrial accidents related to communication technologies - Learning from success stories in industrial safety. **(6hrs)**
Text Books	
	1. "Industrial Safety and Health Management" by C. Ray Asfahl and David W. Rieske
	2. "Principles of Safety" by E. Scott Geller
Reference Books	
	1. "Introduction to Industrial and Systems Engineering" by Wayne C. Turner and Richard D. Ryan
	2. "Safety and Health for Engineers" by Roger L. Brauer
	3. "Introduction to Process Safety for Undergraduates and Engineers" by CCPS (Center for Chemical Process Safety)

M.Tech 2nd Year

SEMESTER-III

MTVLSIC301: Research Methodology & Intellectual Property Rights

Weekly Teaching Hours: - TH: - Tut: -

Scheme of Marking TH: - Tests : - IA: 50 PR/OR: 50 Total : 100

Course Objectives:

The objectives of the course are:

1	To develop an appropriate framework for research studies.
2	To develop an understanding of various research designs and techniques.
3	To develop an understanding of the ethical dimensions of conducting applied research.

Course Outcomes:

At the end of course, students should:

CO1	Understand research problem formulation
CO2	Analyze research related information
CO3	Follow research ethics
CO4	Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
CO5	Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
CO6	Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations**. (7hrs)**

UNIT-II:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, Plagiarism, Research ethics. **(7hrs)**

UNIT-III:

Importance and scientific methodology in recording results, importance of negative results, different ways of recording, industrial requirement, artifacts versus true results, types of analysis (analytical, objective, subjective), outcome as new idea, hypothesis, concept, theory, model. **(7hrs)**

UNIT-IV:

Effective technical writing, how to write a manuscript/ responses to reviewers comments, preparation of research article/ research report, Writing a Research Proposal - presentation and assessment by a review committee. **(7hrs)**

UNIT-V:

Nature of Intellectual Property: Patents, Designs, Trade Mark and Copyright. Process of Patenting and Development: technological research, innovation, patenting & development. Procedure for grants of patents, Patenting under PCT. **(6hrs)**

Unit VI:

Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System, IPR of Computer Software etc. **(6hrs)**

REFERENCES:

1.Kothari, C. R. Research Methodology - Methods and Techniques, New Age International publishers, New Delhi, 2004
2. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
3. Ann M. Korner, Guide to Publishing a Scientific paper, Bioscript Press 2004
4. Mayall, "Industrial Design", McGraw Hill, 1992.
5. Niebel, "Product Design", McGraw Hill, 1974.
6. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

MTVLSIP302: PROJECT-I

Weekly Teaching Hours: -		TH: -	Credit: 10	Tut: -
Scheme of Marking	TH: -	IA: 50	PR/OR: 50	Total : 100

Project-I is an integral part of the final project work. In this, the student shall complete the partial work of the project which will consist of problem statement, literature review, project overview, scheme of implementation that may include mathematical model/SRS/UML/ERD/block diagram/ PERT chart, and layout and design of the proposed system/work. As a part of the progress report of project-I work; the candidate shall deliver a presentation on progress of the work on the selected dissertation topic. It is desired to publish the paper on the state of the art on the chosen topic in international conference/ journal.

The student shall submit the duly certified progress report of project -I in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.

SEMESTER-IV

MTVLSIP401: PROJECT-II

Weekly Teaching Hours: -		TH: -	Credit: 20	Tut: -
Scheme of Marking	TH: -	IA: 100	PR/OR: 100	Total : 200

In Project - II, the student shall complete the remaining part of the project which will consist of the simulation/ analysis/ synthesis/ implementation / fabrication of the proposed project work, work station, conducting experiments and taking results, analysis and validation of results and drawing conclusions.

It is mandatory to publish 02 paper on the state of the art on the chosen topic in reputed international conference/ journal.

The student shall prepare the duly certified final report of project work in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.